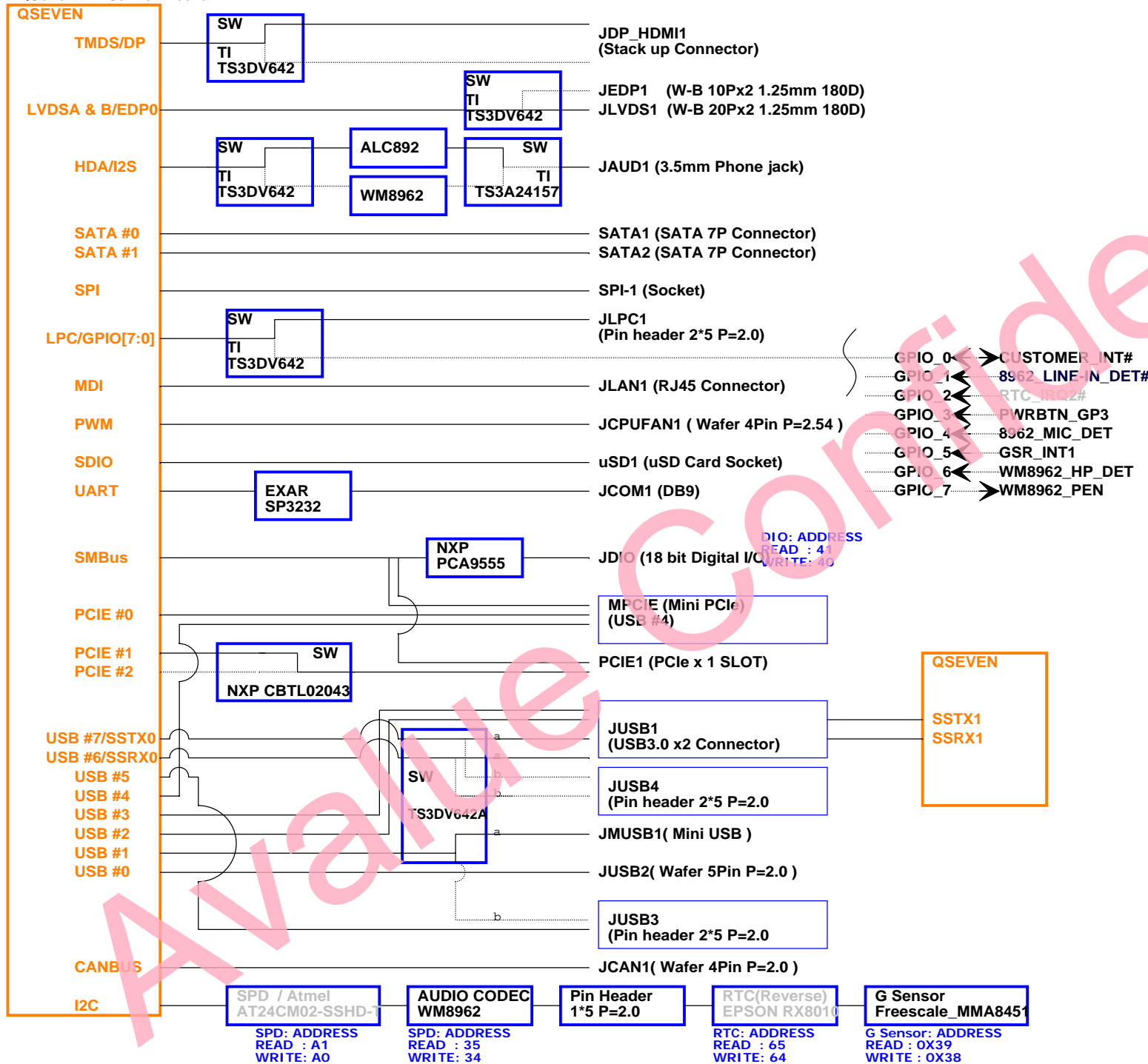


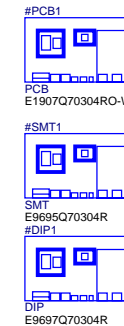
REV-Q703 B1 Block diagram

QSeven 2.1 Carrier Board



Cover Sheet:

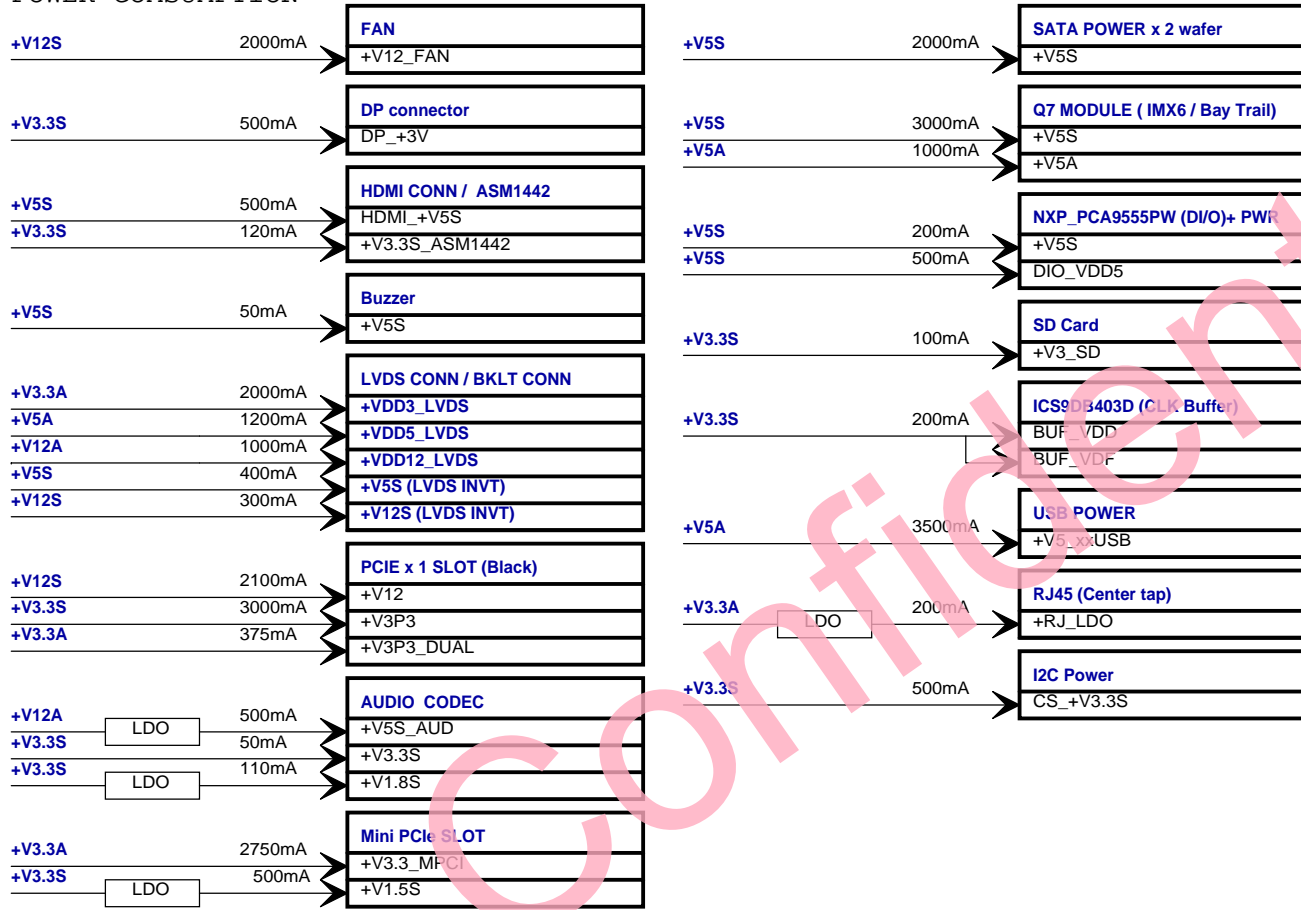
01. Cover Sheet / Block Diagram
02. Power Delivert Map, Reset Map
03. Power on squence
04. DP_TMDS_SWITCH / FUNC SEL
05. DP CONN
06. HDMI CONN
07. LVDS & EDP CONN
08. SATA/SPI/DIO/uSD/SPD
09. PCIE CLOCK BUFFER / COM PORT
10. MINI PCIE SLOT/ +V1.5S
11. PCIe x1 SLOT
12. USB 2.0 / 3.0 SW
13. USB 3.0 x2 / USB 2.0 x 6
14. RJ45 / Mini USB
15. Q7 Connector
16. Front Panel / WDT
17. LPC_GPIO_SWITCH
18. PWR OK / FAN / LPC / RTC
19. V12S, V5S, V3.3S/G Sensor/CAN
20. TPS51220A +V5A & +V3.3A
21. DC 12 Vin / Discharge
22. HDA & I2S Switch
23. AUDIO ALC892 / Buzzer
24. AUDIO WM8962
25. AUDIO PHONE JACK
26. History



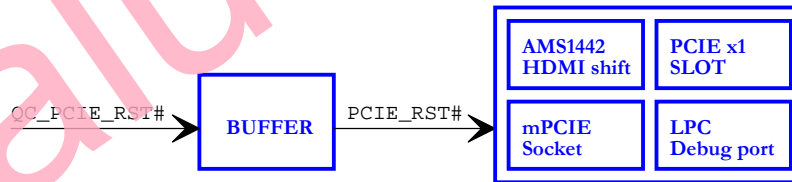
avalue Technology Inc.		Confidential	
Project Name	REV-Q703	Module Number	<Module no.> ?
Size	Custom	Title	Cover Sheet / Block Diagram
Date:	Thursday, February 09, 2017	Sheet	1 of 26

Power Delivery Map

POWER CONSUMPTION



RESET MAP



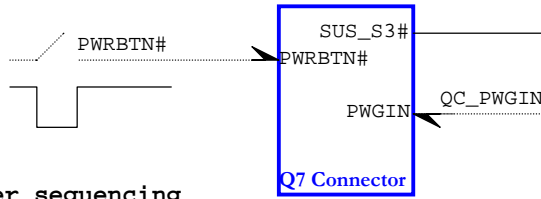
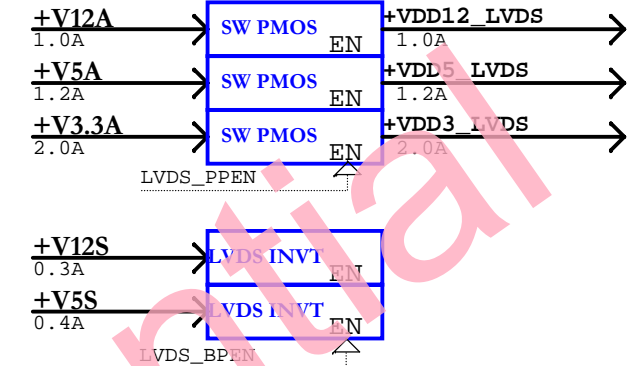
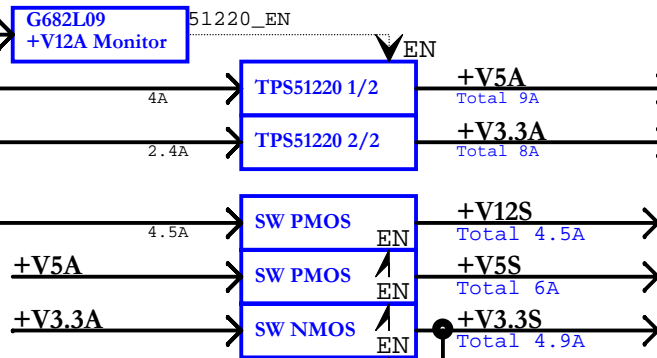
Power on sequence

DC IN 12V
12A

LM5069
UVP
OVP
V Limit
I Limit

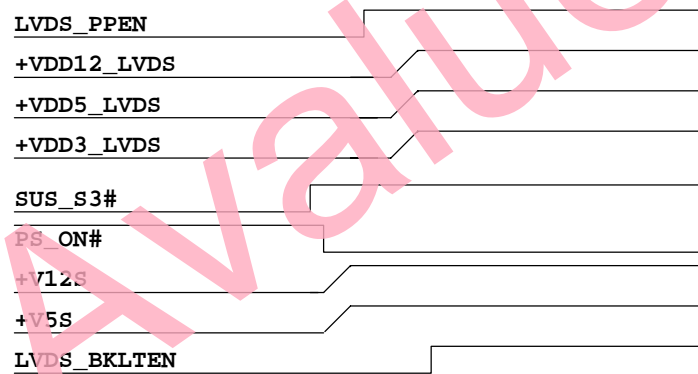
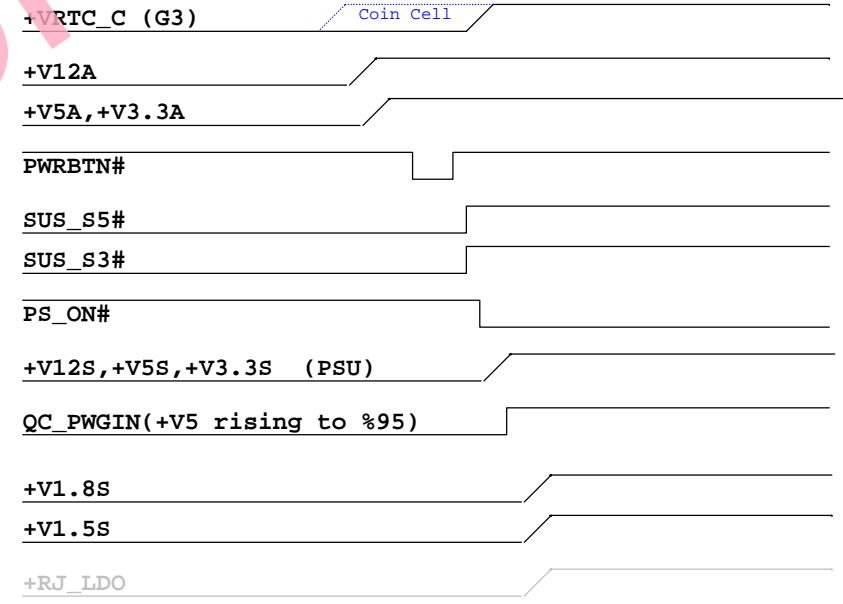
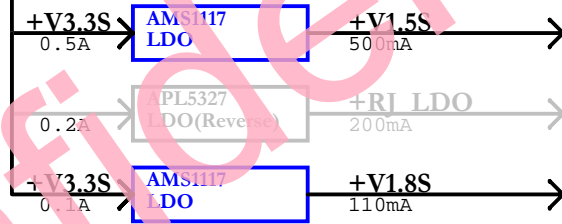
+V12A
Total 11A

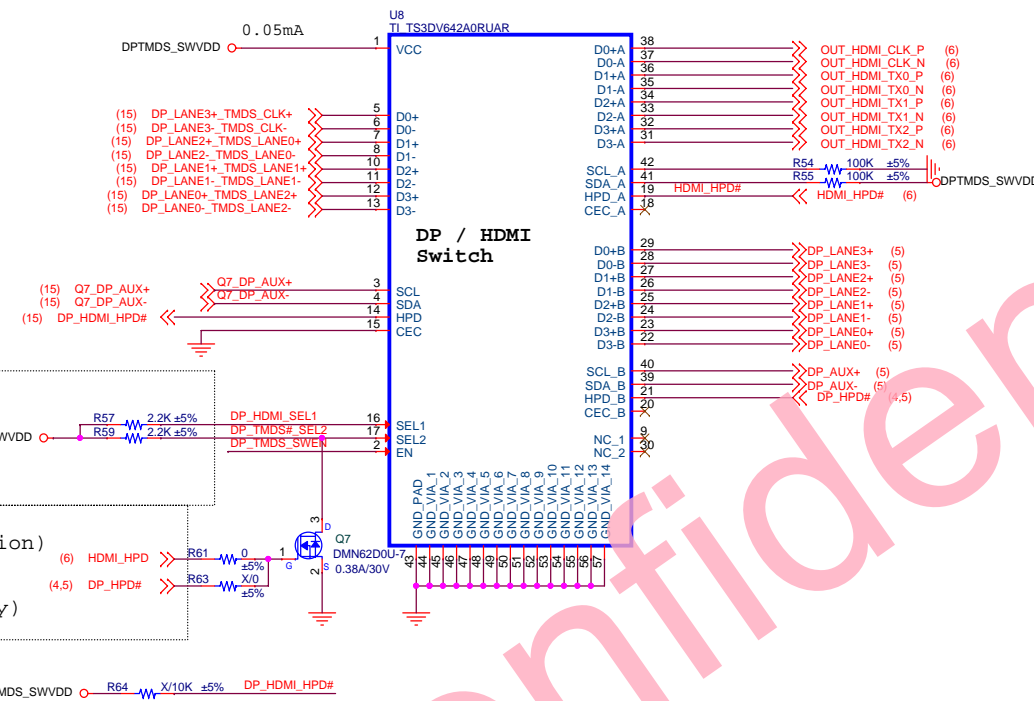
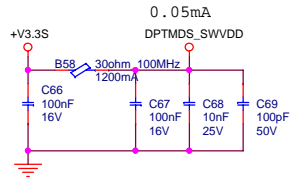
I LIM(min) is 9.7A
I LIM(typ) is 11.1A
I LIM(max) is 12.3A
116.4W - 133.2W - 147.6W



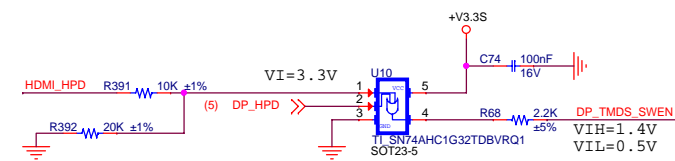
Qseven input power sequencing requirements are as follows:

- +VRTC rise to +V5A >=0ms
- +V5A rise to +V5S >=0ms
- +V5S VCC rise to 95% to PWGIN >=0ms





Pin17 input logic (Auto selection)
 DP vs HDMI ,Pin17 SEL2
 HI , DP OUTPUT.
 LOW, HDMI OUTPUT.(High Priority)



When insert HDMI or DP cable
 switch IC enable.

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0- to D0+A/D0-A ON. All the other channels Hi-Z.
H	L	H	D0+/D0- to D0+B/D0-B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

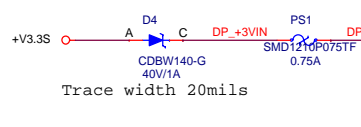
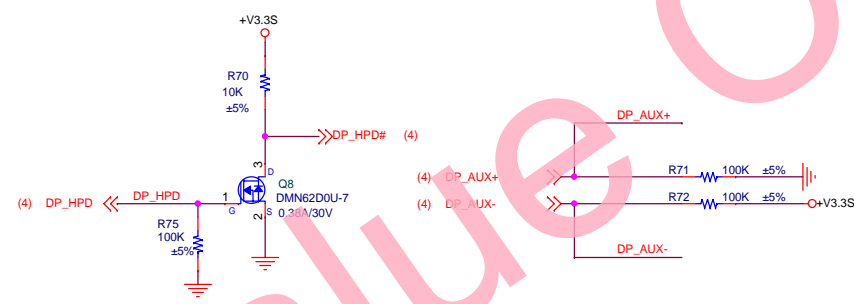
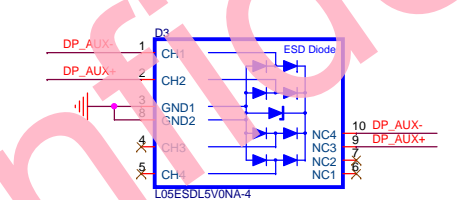
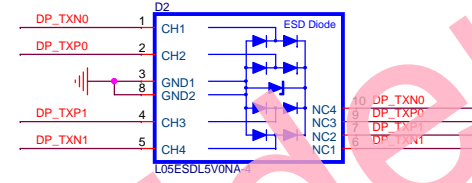
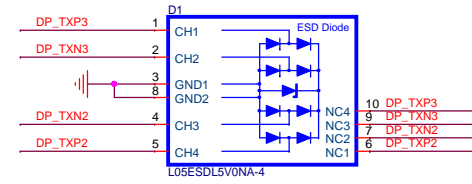
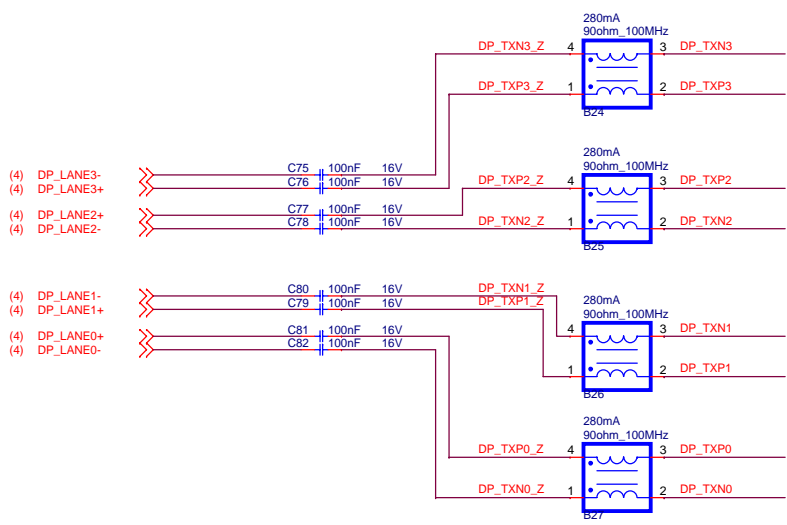
Use all channel.

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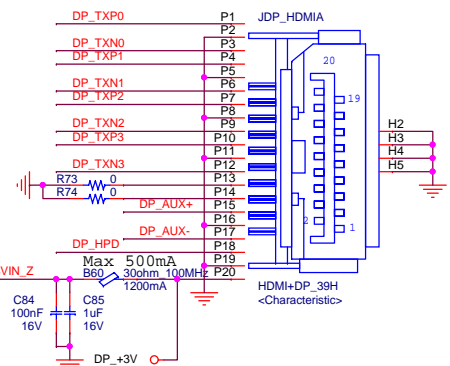
Project Name: **REV-Q703** Module Number: **<Module no.>** Rev: **?**

Size: **A3** Title: **DP_TMDS_SWITCH** Rev: **B1**

Date: **Thursday, February 09, 2017** Sheet: **4** of **26**

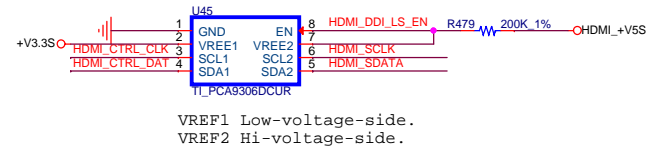
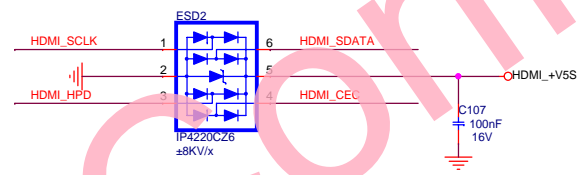
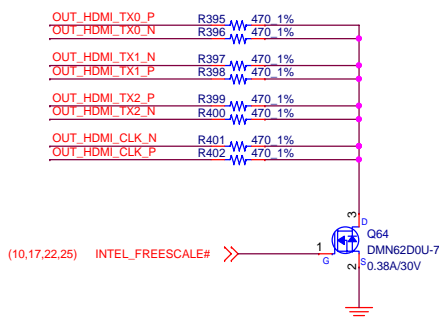
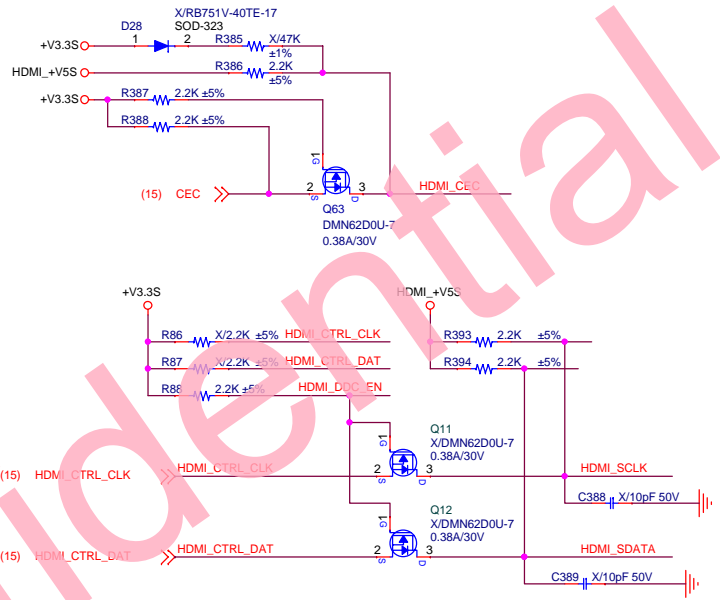
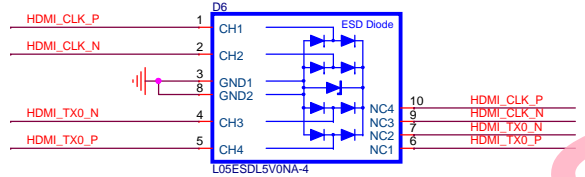
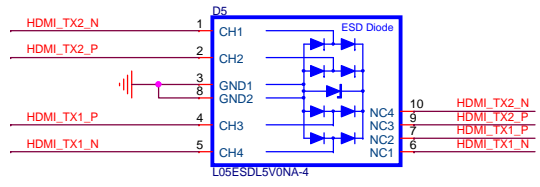
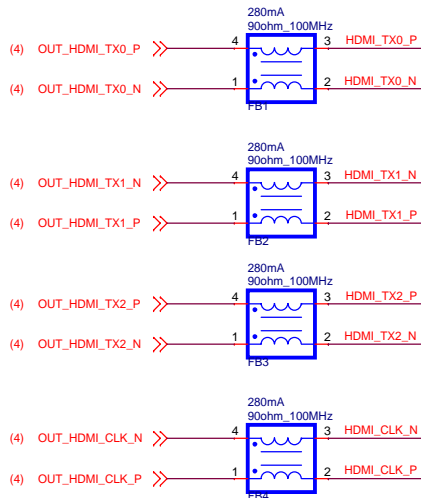


DP CONN

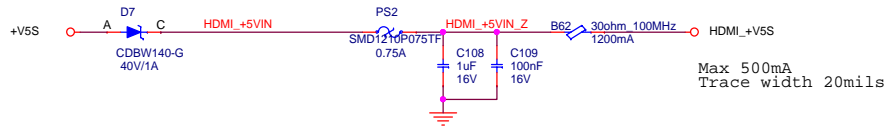
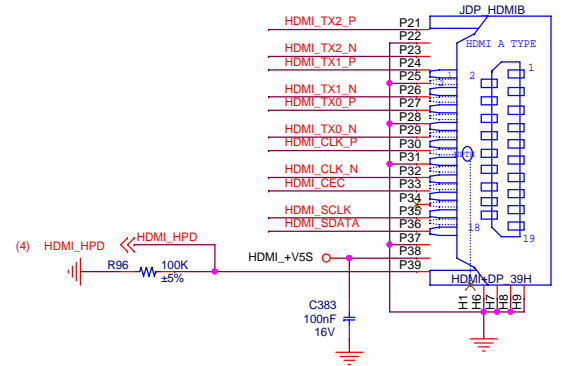
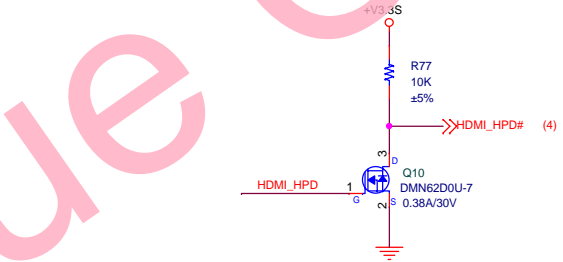
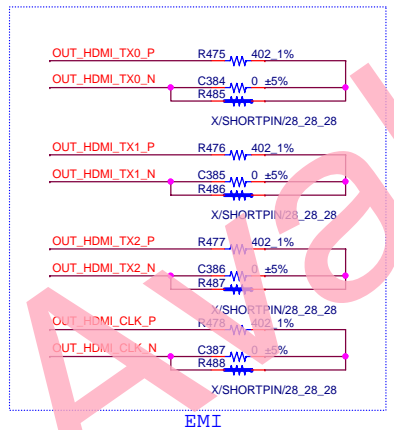


Available Confidential

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Project Name	REV-Q703	Module Number	<Module no.>
Size	A3	Title	DP Connector
Date:	Thursday, February 09, 2017	Sheet	5 of 26

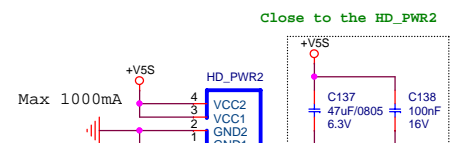
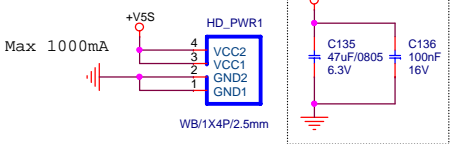
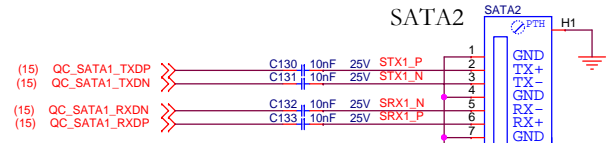
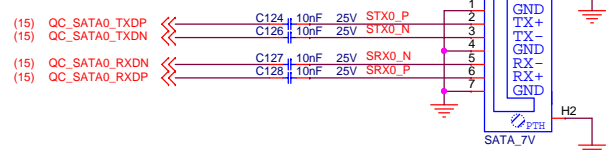


HDMI CONN



avalue Technology Inc.		Confidential	
Project Name	REV-Q703	Module Number	<Module no.>
Size A3	Title HDMI CONN	Rev	?
Date	Friday, February 17, 2017	Sheet	6 of 26

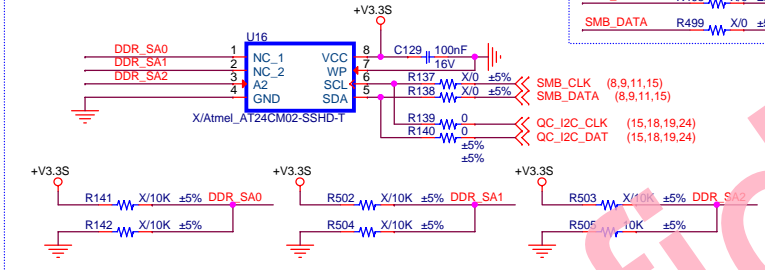
SATA



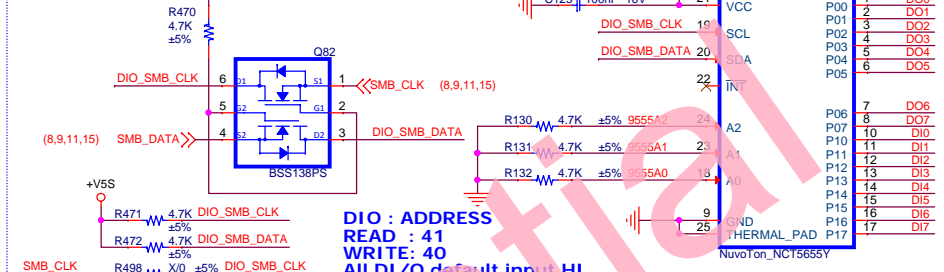
I2C EEPROM 2Mbit REVERSE

Table 4-1. Device Address Byte

Package Type	Device Type Identifier				Hardware Address Bit	MSB Address Bits			Read/Write
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SOIC, WLCSOP	1	0	1	0	A ₇	A ₁₇	A ₁₆	R/W	

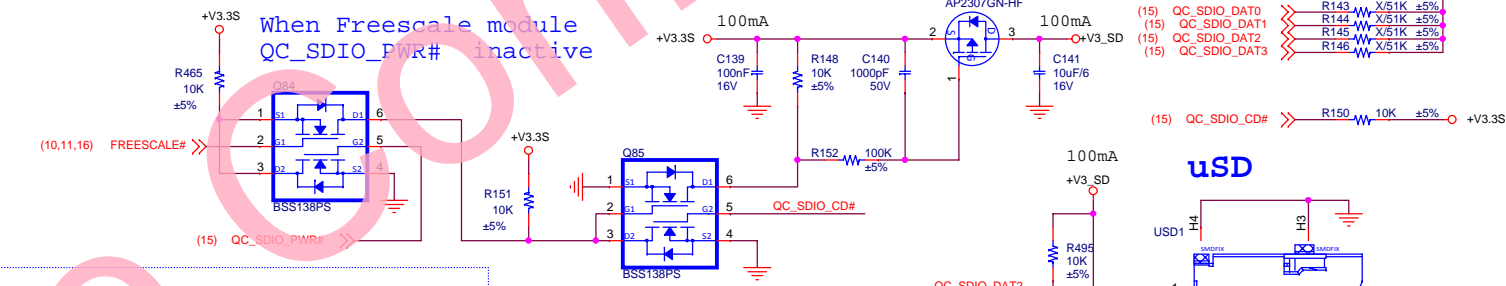


DIO8*8

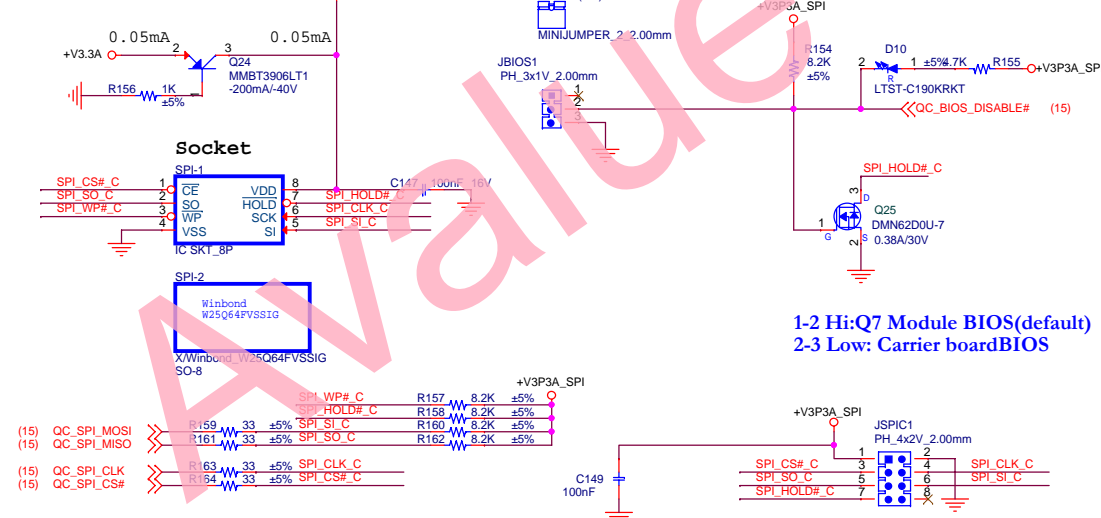


DIO : ADDRESS
READ : 41
WRITE: 40
All DI/O default input HI

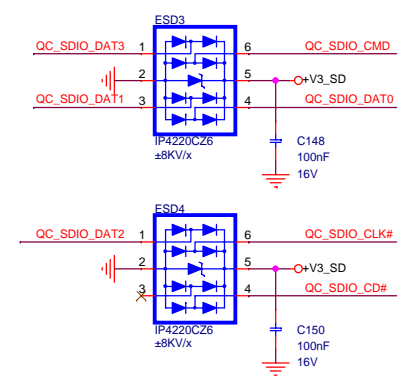
uSD CARD



SPI



1-2 Hi: Q7 Module BIOS (default)
2-3 Low: Carrier board BIOS



Card detection switch		Write protection switch	
When card is ejected	When card is inserted	When card is ejected	When card is inserted
Write protect	Write enable	Write protect	Write enable
<input type="checkbox"/> OPEN <input type="checkbox"/> CLOSE	<input type="checkbox"/> OPEN <input type="checkbox"/> CLOSE	<input type="checkbox"/> OPEN <input type="checkbox"/> CLOSE	<input type="checkbox"/> OPEN <input type="checkbox"/> CLOSE
Sb Sc	Sa Sc	Sa Sc	Sa Sc

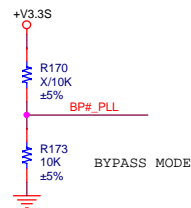
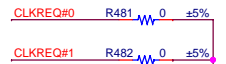
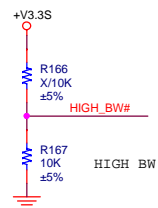
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Project Name: **REV-Q703** Module Number: **<Module No.>** Rev: **?**

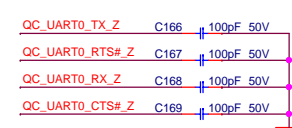
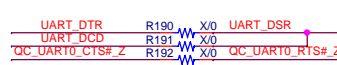
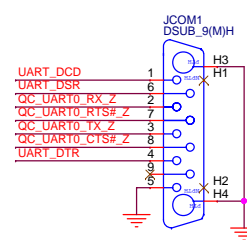
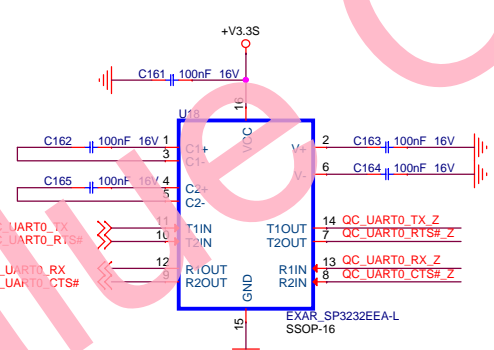
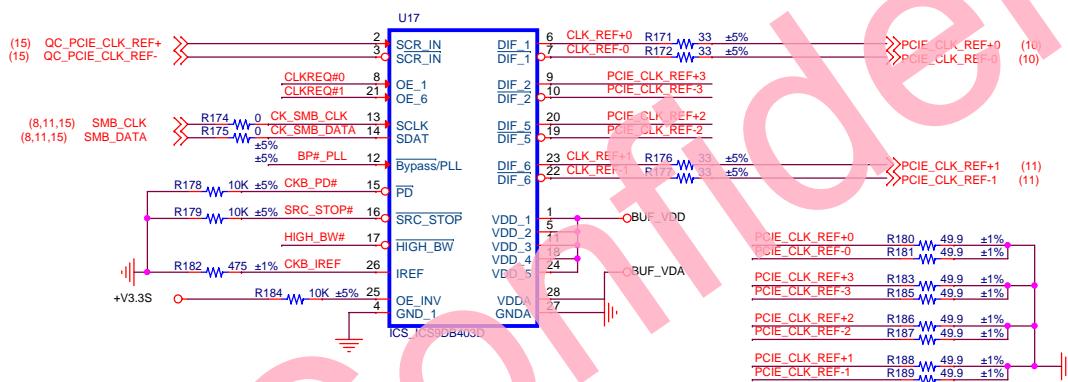
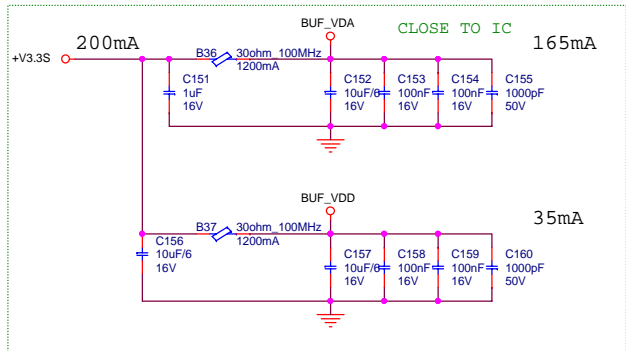
Size A3 Title: **SATA/SPI/DIO/uSD/SPD** Rev: **B1**

Date: Thursday, February 09, 2017 Sheet: 8 of 26

PCIe Clock Buffer

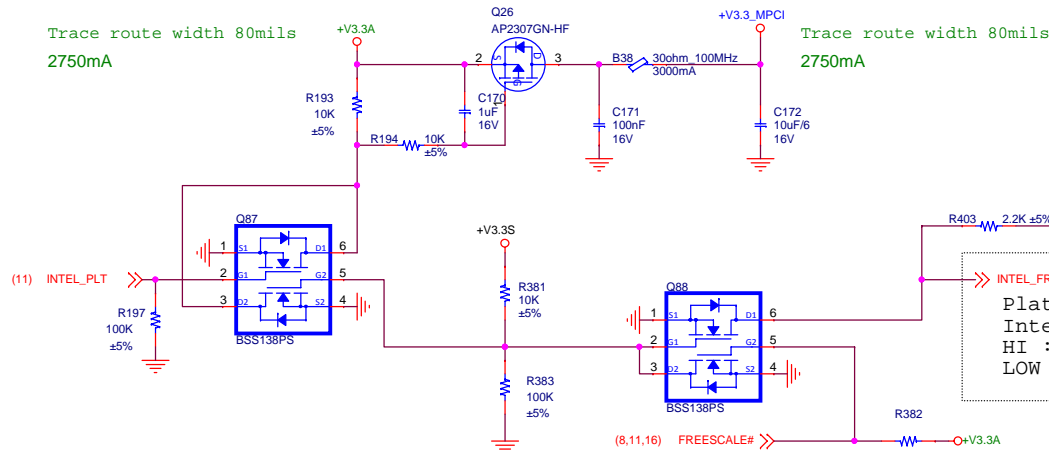


When OE_INV = 1
OE1#=Low active.
OE6#=Low active.
SRC_STOP=High active.
PD=High active.



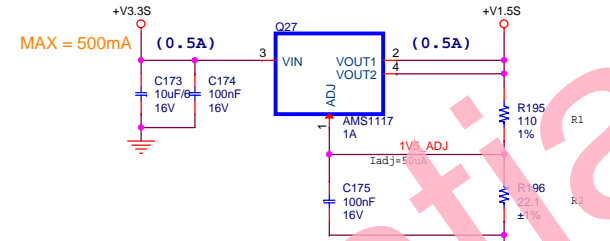
While the normal PC hardware might well run with just Tx, Rx and Ground connected, most driver software will wait forever for one of the handshaking lines to go to the correct level. Depending on the signal state it might sometimes work, other times it might not. The reliable solution is to loop back the handshake lines if they are not used.

Trace route width 80mils
2750mA



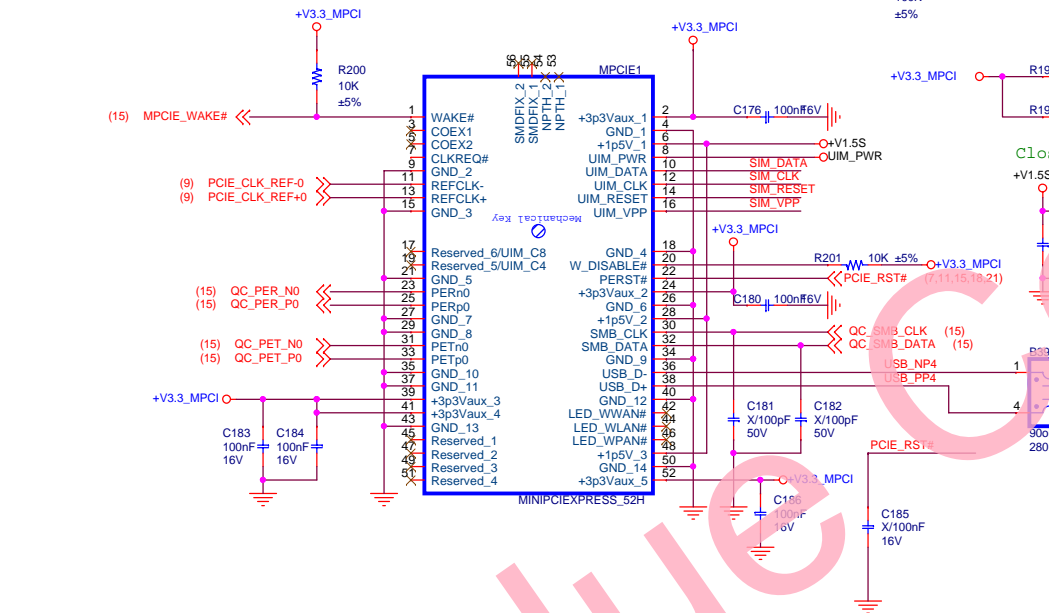
+V1.5S Power

Trace route width 20mils

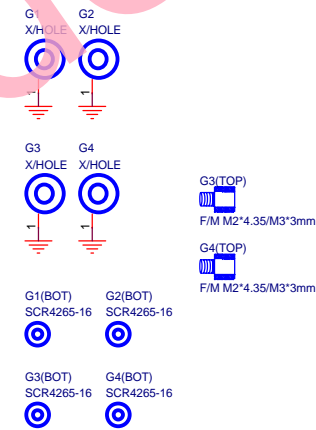


minimux load 10mA
 $V_{OUT} = V_{REF} (1 + R2/R1) - I_{ADJ}R2$
 $= 1.25 * [1 + (R2/R1)] - I_{ADJ}R2 = 1.502V$

LDO: +V3.3S to +V1.5S - 500mA

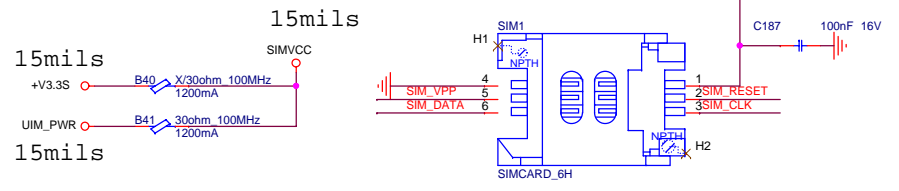


Platform SELECTION
 Intel VS Freescale
 HI : Intel
 LOW : Freescale



Power Rail	Voltage Tolerance	D0-D2, D3 ^{hot} Power ¹		D3 ^{cold} Power ^{2,3}	
		Peak (max) mA	Normal (max) mA	Peak (max) mA	Normal (max) mA
3.3Vaux	±9%	2,750	1,100	2,750 (wake enabled)	250 (wake enabled)
+1.5V	±5%	500	375	N/A	N/A

SIM Card Push Push

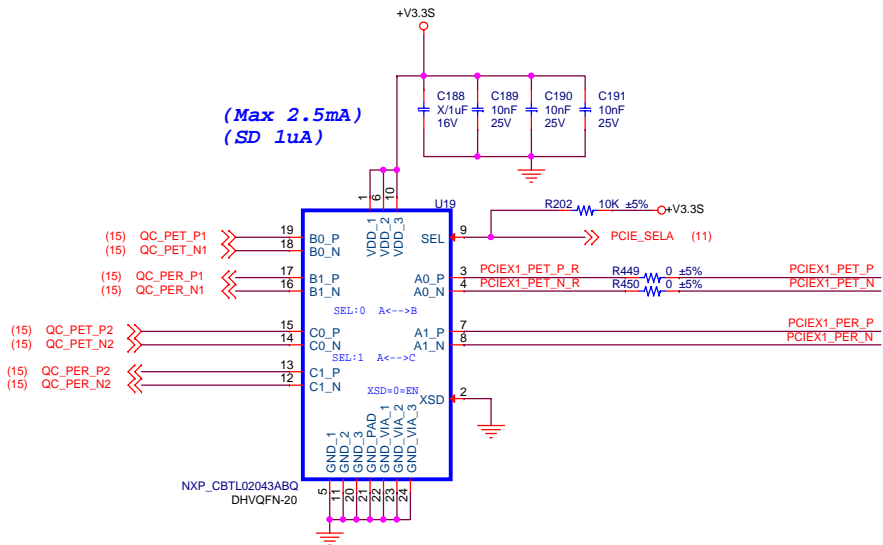


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Project Name	REV-Q703	Module Number	<Module no.>	Rev	?
Size	A3	Title	MINI PCIE SLOT/ +V1.5S	Rev	B1
Date:	Thursday, February 09, 2017	Sheet	10	of	26

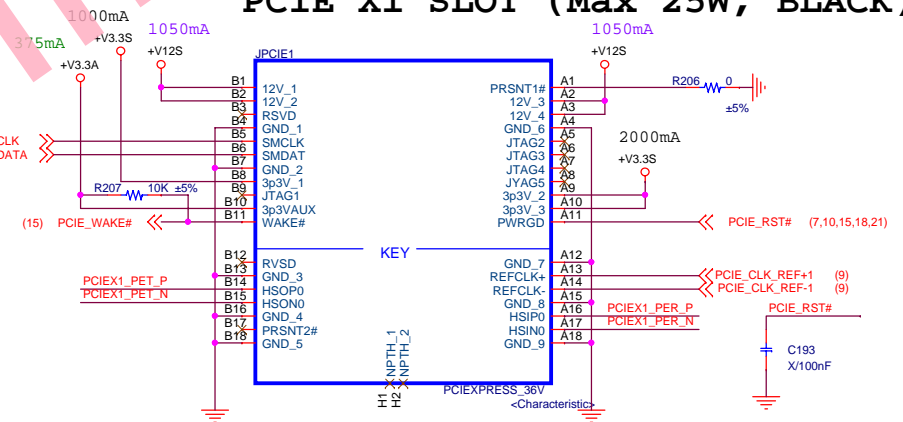
PCIE PORT SWITCH

(Max 2.5mA)
(SD 1uA)



SEL	9	12	CMOS single-ended input	operation mode select SEL = LOW: A ↔ B SEL = HIGH: A ↔ C
XSD	2	19	CMOS single-ended input	Shutdown pin; should be driven LOW or connected to V _{SS} for normal operation. When HIGH, all paths are switched off (non-conducting high-impedance state), and supply current consumption is minimized.

PCIE X1 SLOT (Max 25W, BLACK)



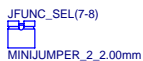
AT and ATX Mode SELECTION

AT mode VS ATX mode
SHORT 1-2 : For AT mode (default); OPEN 3-4
SHORT 3-4 : For ATX mode; OPEN 1-2



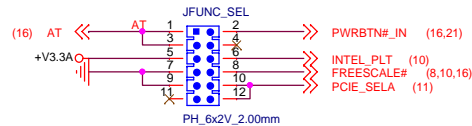
Platform SELECTION

Intel VS Freescale
SHORT 5-6 : For Intel platform; OPEN 7-8
SHORT 7-8 : For Freescale platform(default) OPEN 5-6

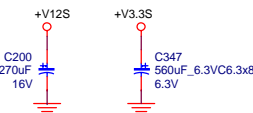
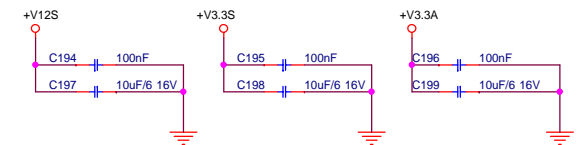


PCIe channel selection

PCIe1 VS PCIe2
SHORT 9-10 : For PCIe1 (default); OPEN 11-12
SHORT 11-12 : For PCIe2; OPEN 9-10



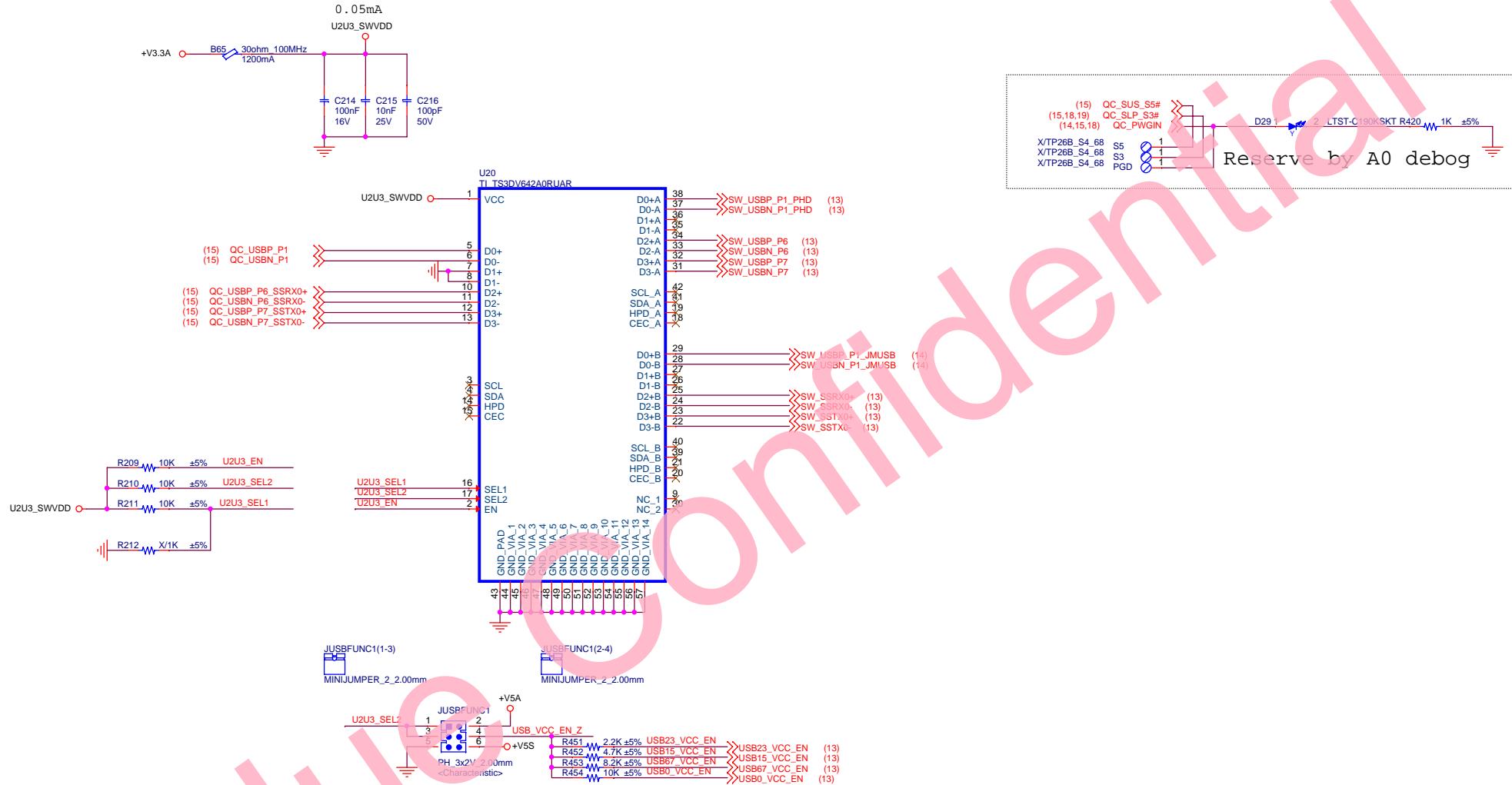
Closed to Connector



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Project Name	REV-Q703	Module Number	<Module no.>	Rev	?
Size	A3	Title	PCIe x1 SLOT/ FUNC SEL	Rev	B1
Date:	Thursday, February 09, 2017	Sheet	11	of	26

USB 2.0 / 3.0 Switch



JUSBFUNC1 SELECTION

SHORT1-3: Port 1,6,7 to B(Mini USB & USB3.0 CONN, default). Used JMUSB1 & JUSB1(USB3.0) or
 SHORT3-5: Port 1,6,7 to A(USB 2.0 x1 & USB 2.0 x1 pin header) . Used JUSB3 & JUSB4

SHORT 2-4 : It provided standby power to USB. (default)

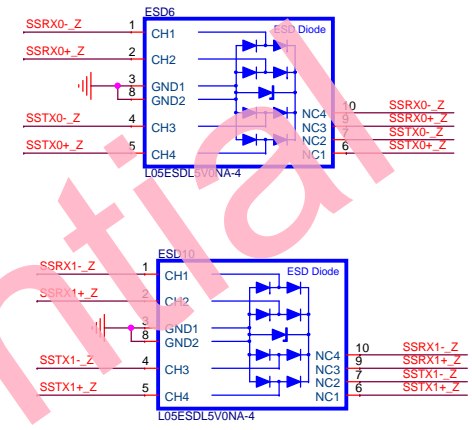
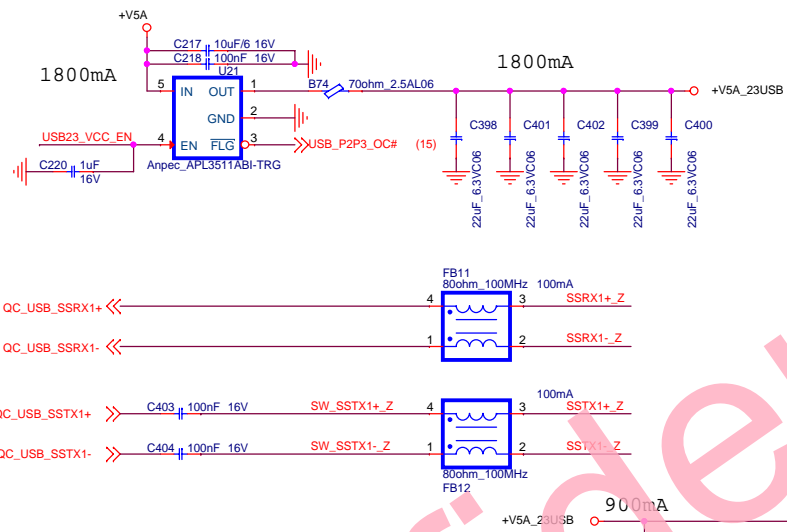
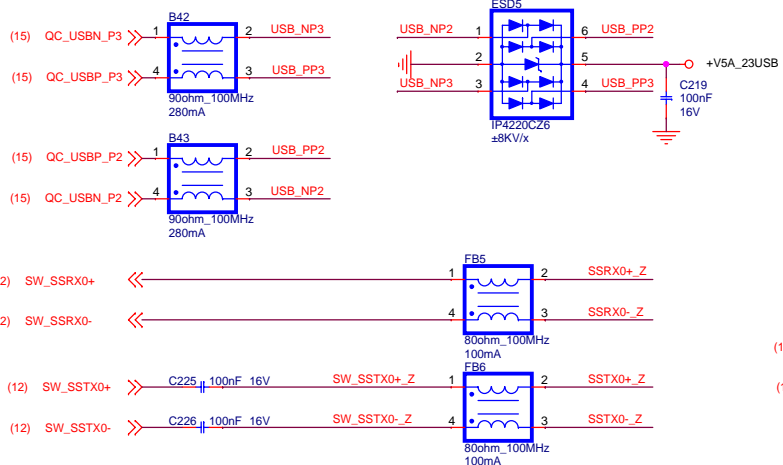
SHORT 4-6 : It provided USB power when main power ok.

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0- to D0+A/D0-A ON. All the other channels Hi-Z.
H	L	H	D0+/D0- to D0+B/D0-B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

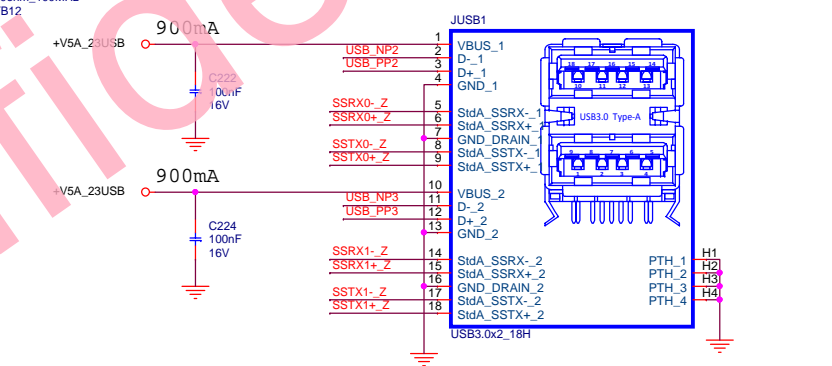
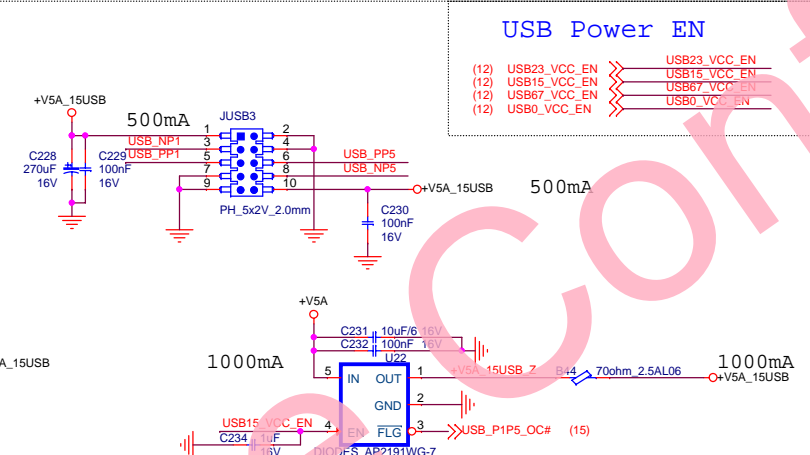
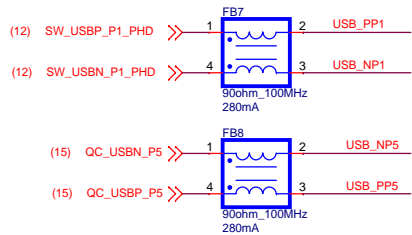
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Project Name	REV-Q703	Module Number	<Module no.>	Rev	?
Size	A3	Title	USB 2.0 / 3.0 SWITCH	Rev	B1
Date:	Thursday, February 09, 2017	Sheet	12	of	26

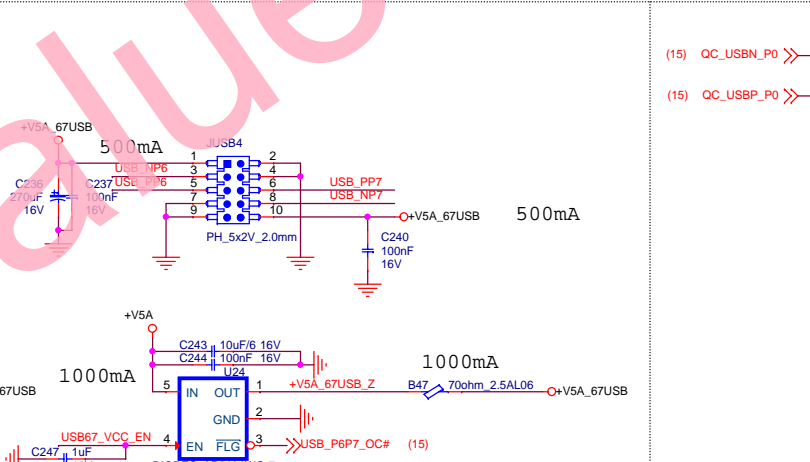
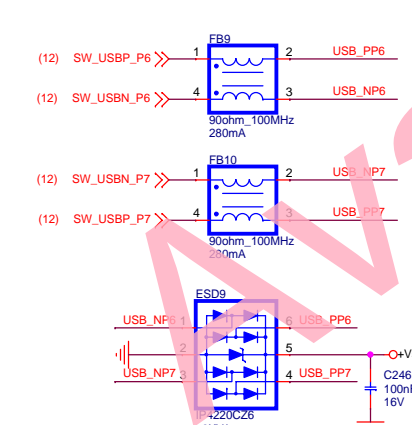
USB 3.0 x 1 / USB 2.0 X 1



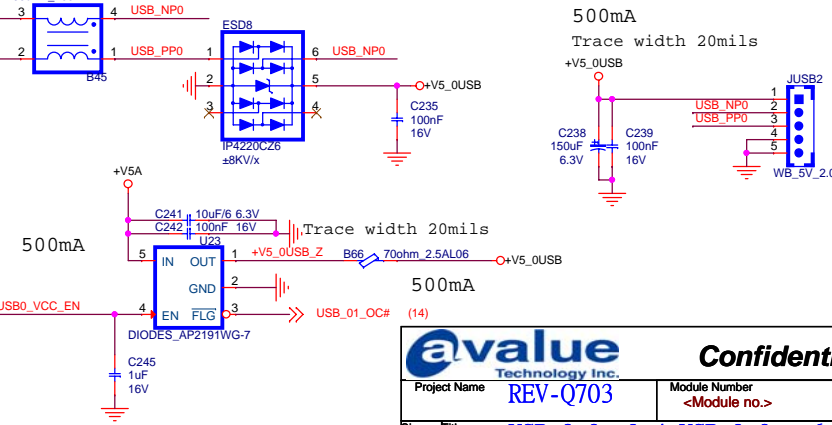
USB 2.0 x 2



USB 2.0 x 2



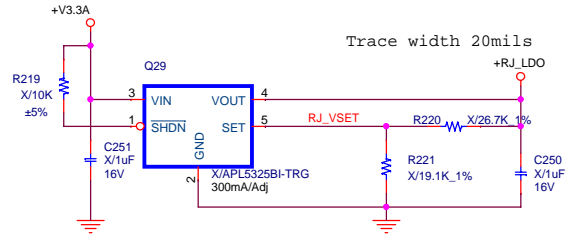
USB 2.0 x 1 (for TOUCH FUNCTION)



a value
 Technology Inc.
Confidential
 Project Name **REV-Q703** Module Number **<Module no.>** Rev ?
 Size A3 Title **USB 3.0 x2 / USB 2.0 x 6** Rev B1
 Date: Thursday, February 09, 2017 Sheet 13 of 26

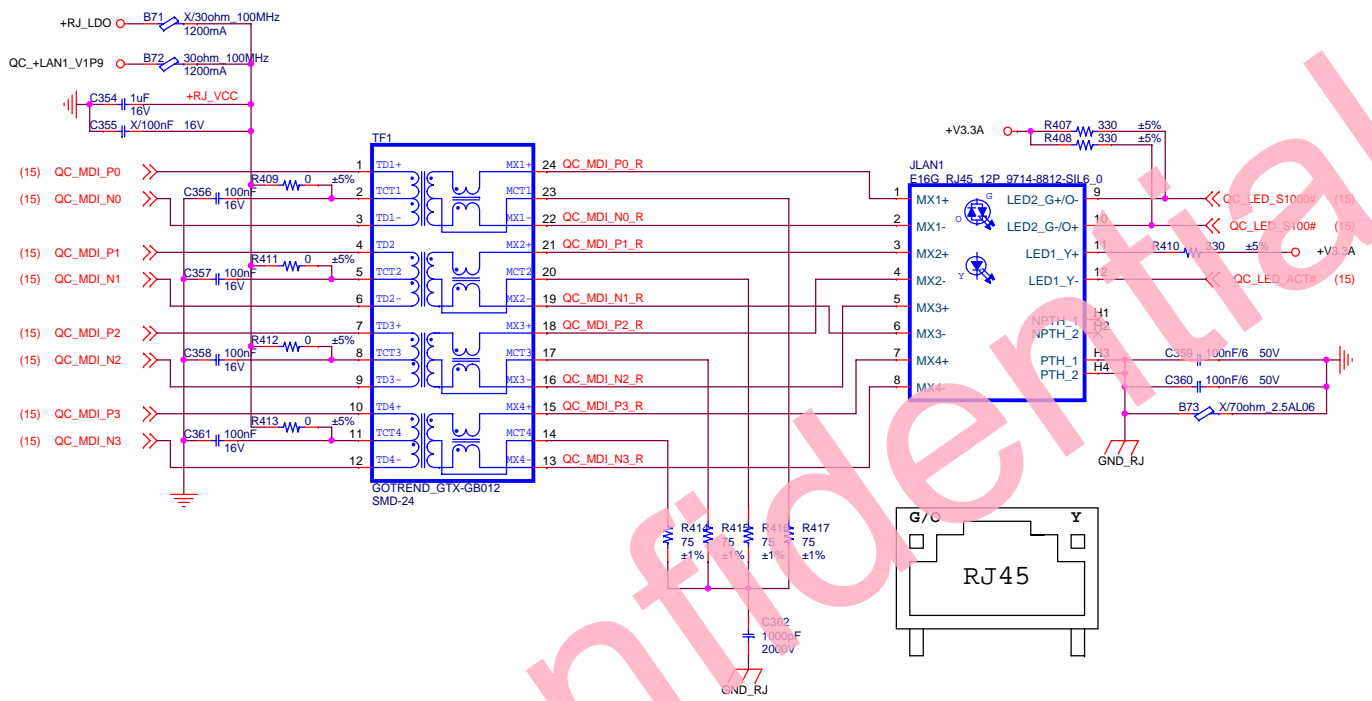
RJ45

Trace width 20mils

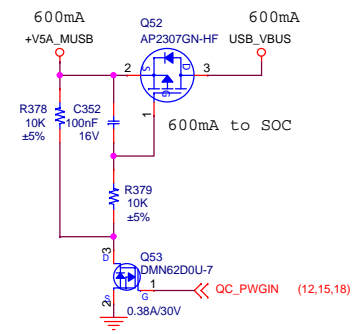
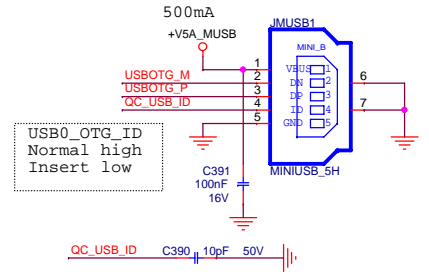
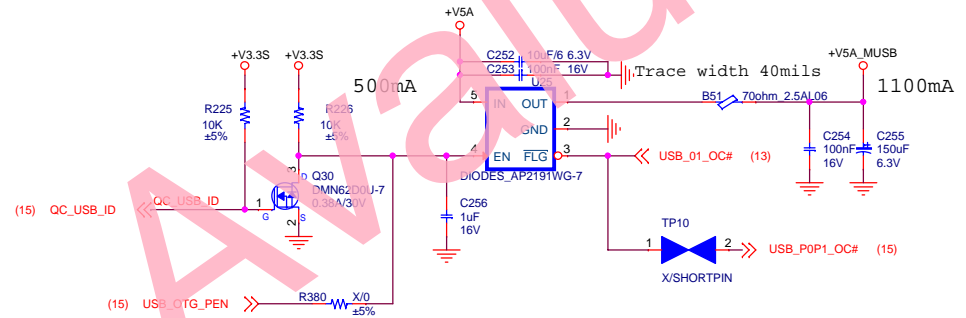
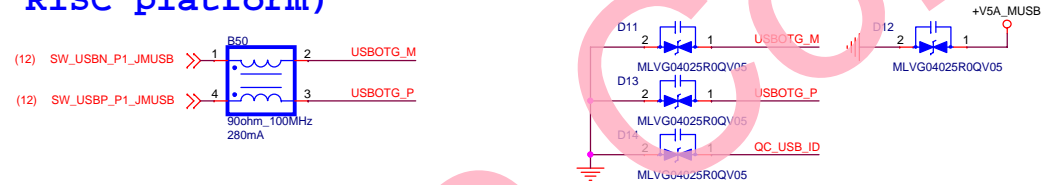


$$V_{out} = 0.8 [1 + (R_{up}/R_{dn})] = 1.918V$$

When $R_{up} = 6.04k$, $V_{out} = 1.92V$

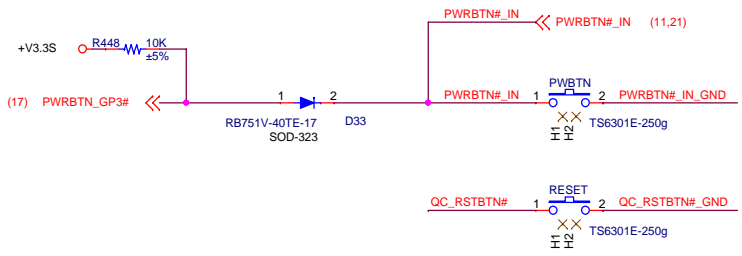
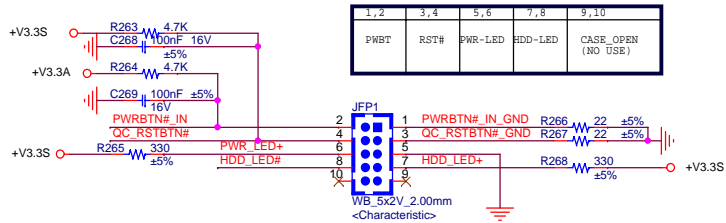


USB OTG (For RISC platform)

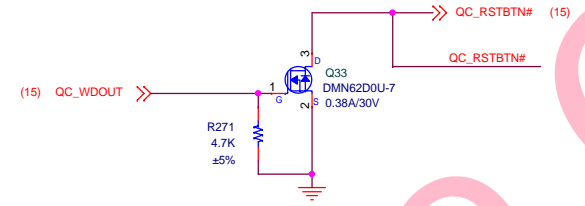


avalue Technology Inc.		Confidential	
Project Name	REV-Q703	Module Number	<Module no.>
Size A3	Title RJ45 / Mini USB	Rev B1	?
Date:	Thursday, February 09, 2017	Sheet	14 of 26

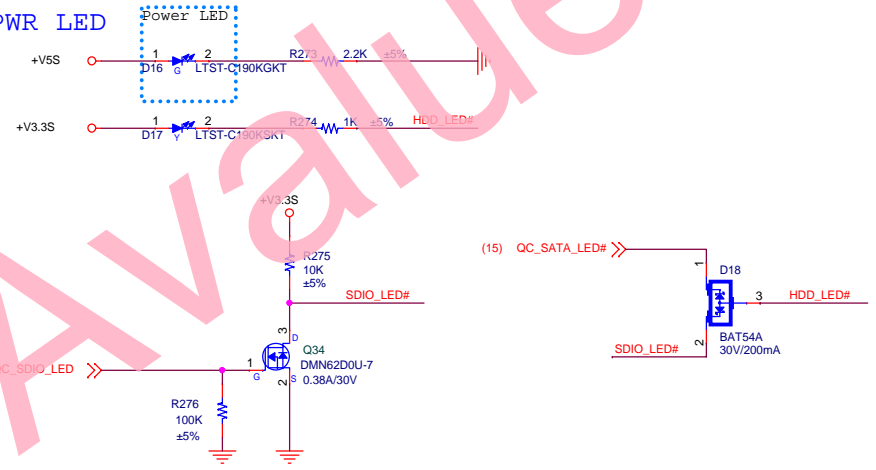
Front Panel



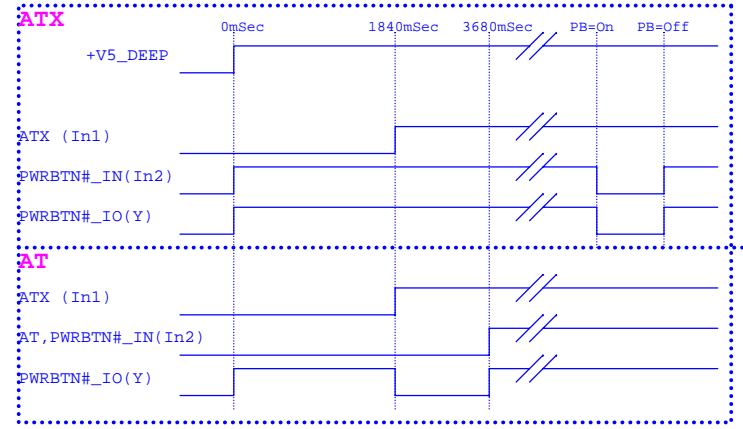
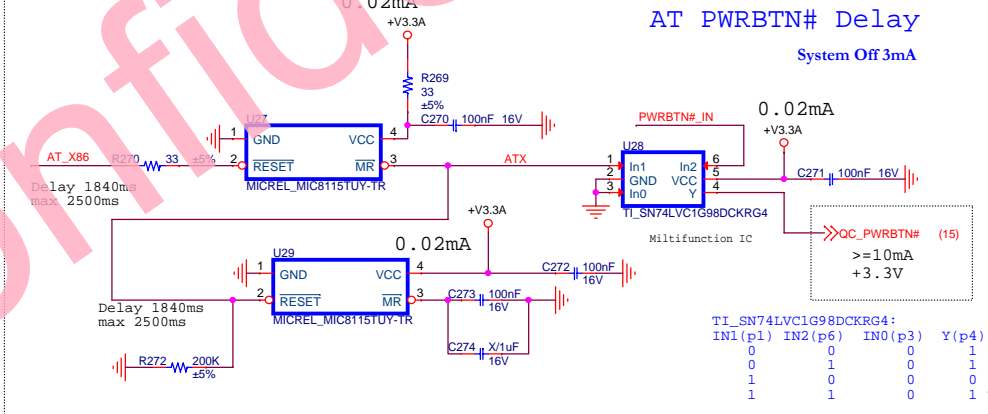
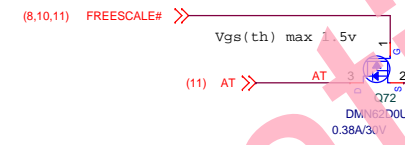
WDT

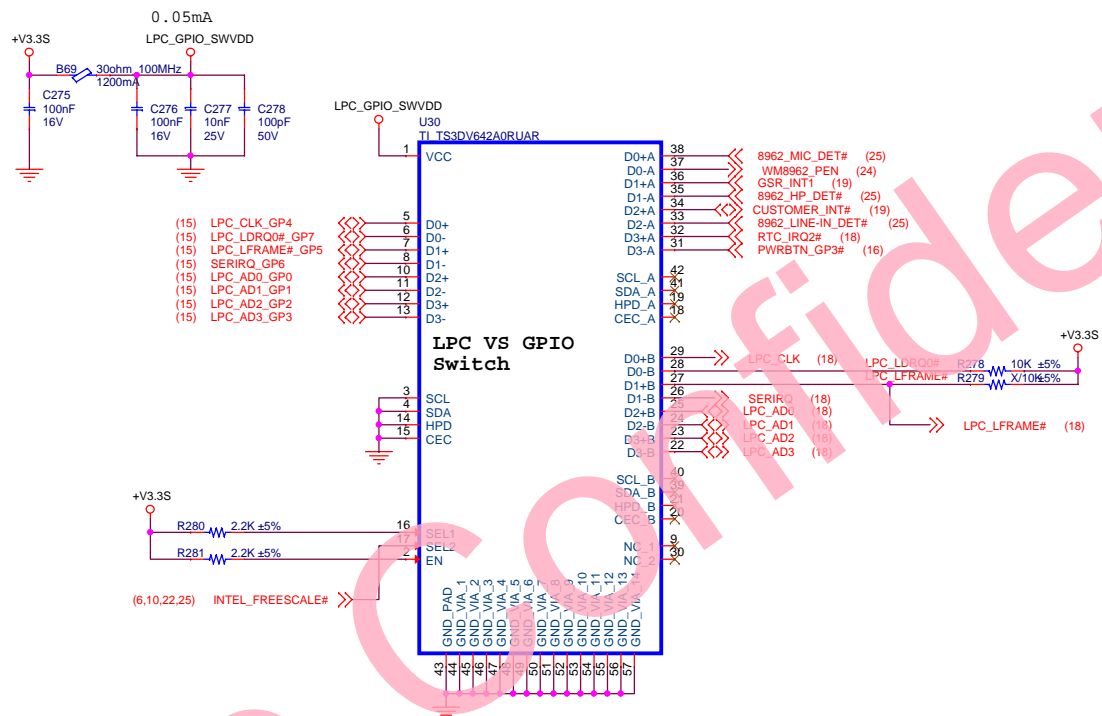


HDD LED / PWR LED



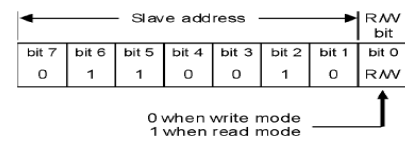
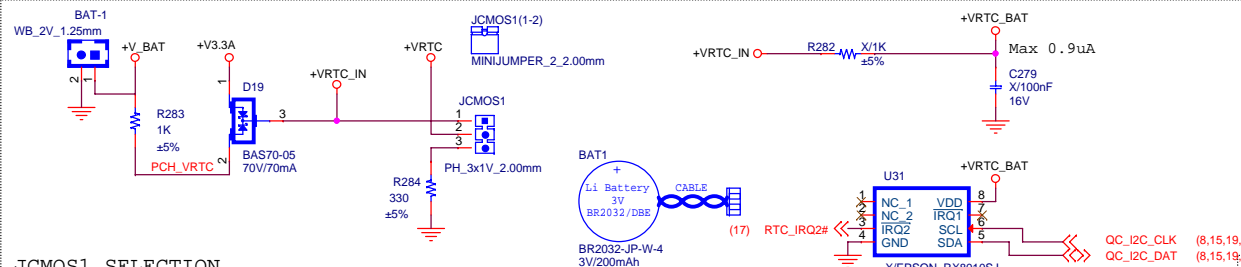
When Freescale module AT Mode auto power button inactive





Use all channel.

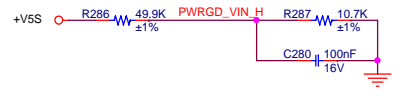
EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0- to D0+A/D0-A ON. All the other channels Hi-Z.
H	L	H	D0+/D0- to D0+B/D0-B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.



RTC CHIP: ADDRESS
 READ : 65
 WRITE: 64

JCMOS1 SELECTION
 SHORT 1-2 : Normal.
 SHORT 2-3 then SHORT 1-2 : Clear CMOS.

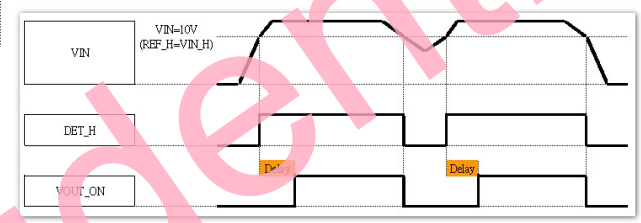
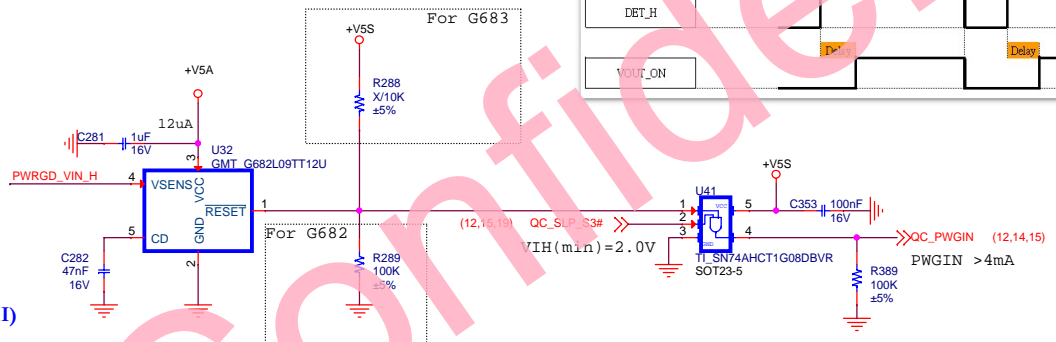
Q7 carrier board POK



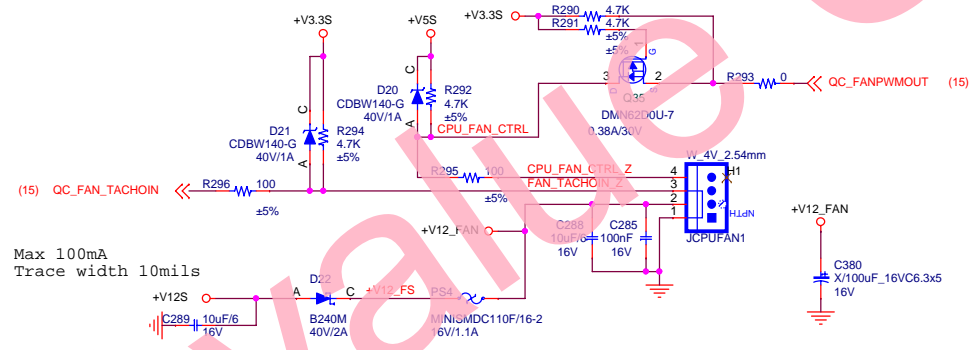
$$t_{RP} \text{ (ms)} = 2.7 \times CD \text{ (nF) at } V_{CC} = 3.3V$$

$$\approx -127ms$$

VSENS(Reset threshold 0.788V)
 $= V_{in} \cdot R_{dn} / (R_{up} + R_{dn})$
 $= VSENS \cdot (R_{up} + R_{dn}) / R_{dn}$
 $= 4.46V$ (When +V5S_C rising 94.4% output HI)

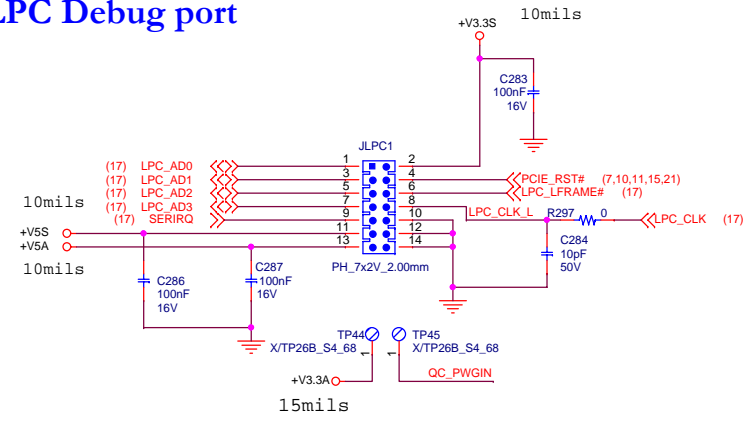


CPU Fan

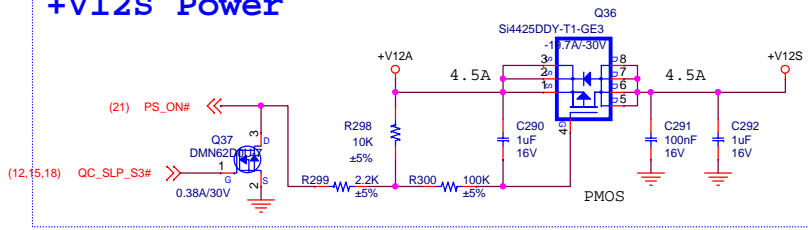


Max 100mA
 Trace width 10mils

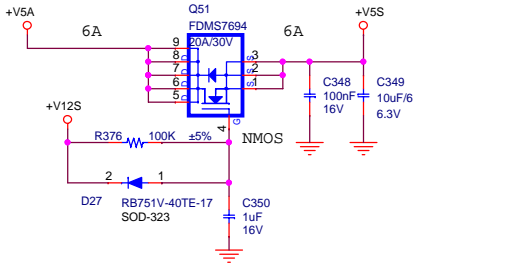
LPC Debug port



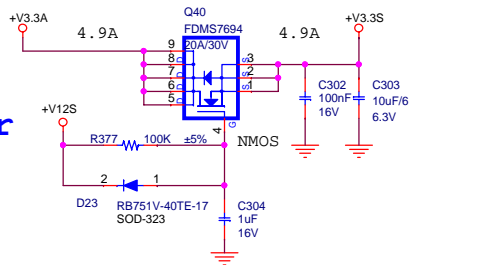
+V12S Power



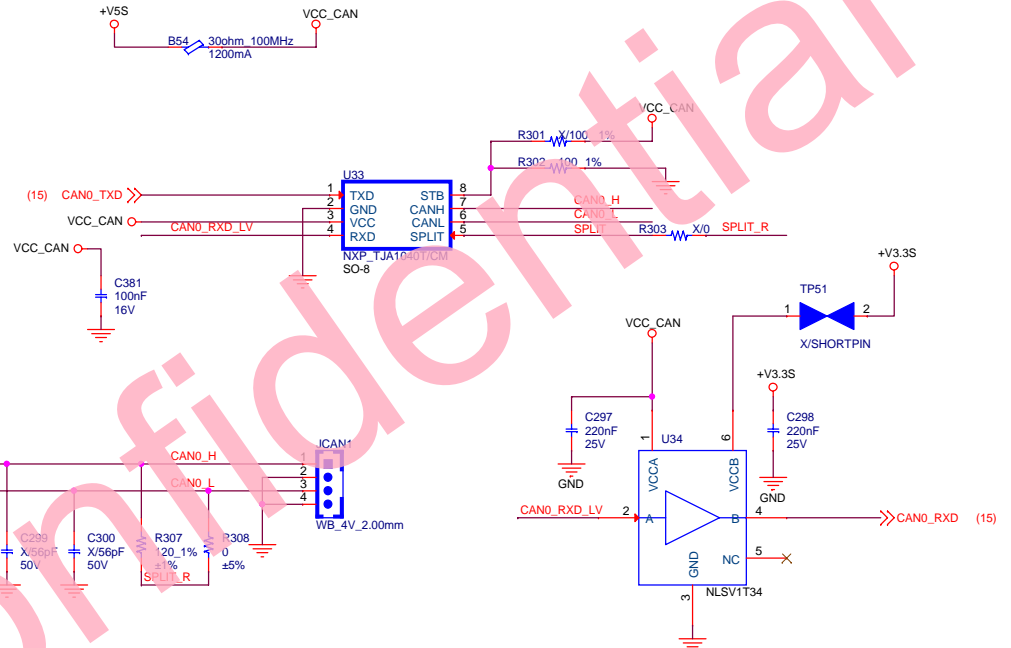
+V5S Power



+V3.3S Power



CAN bus



If use SPLIT : R307 60ohm, R308 60ohm.
If no use : R307 120ohm , R308 0ohm

G Sensor

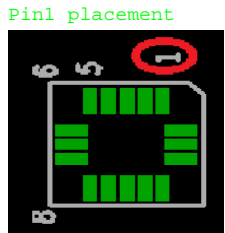
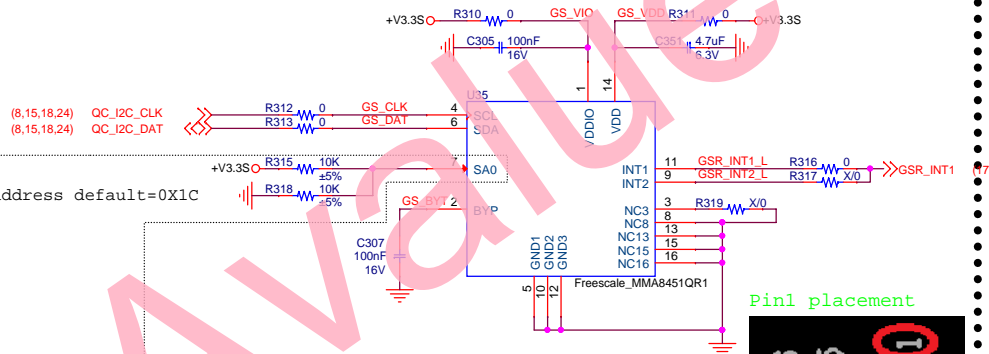
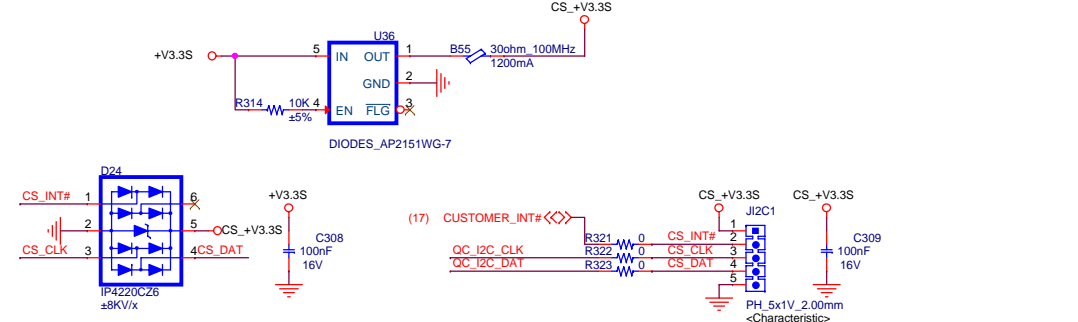


Table 10. I²C Address Selection Table

Slave Address (SA0 = 0)	Slave Address (SA0 = 1)	Comment
0011100 (0x1C)	0011101 (0x1D)	Factory Default

G Sensor: ADDRESS
READ : 0X39
WRITE : 0X38

Customer I2C



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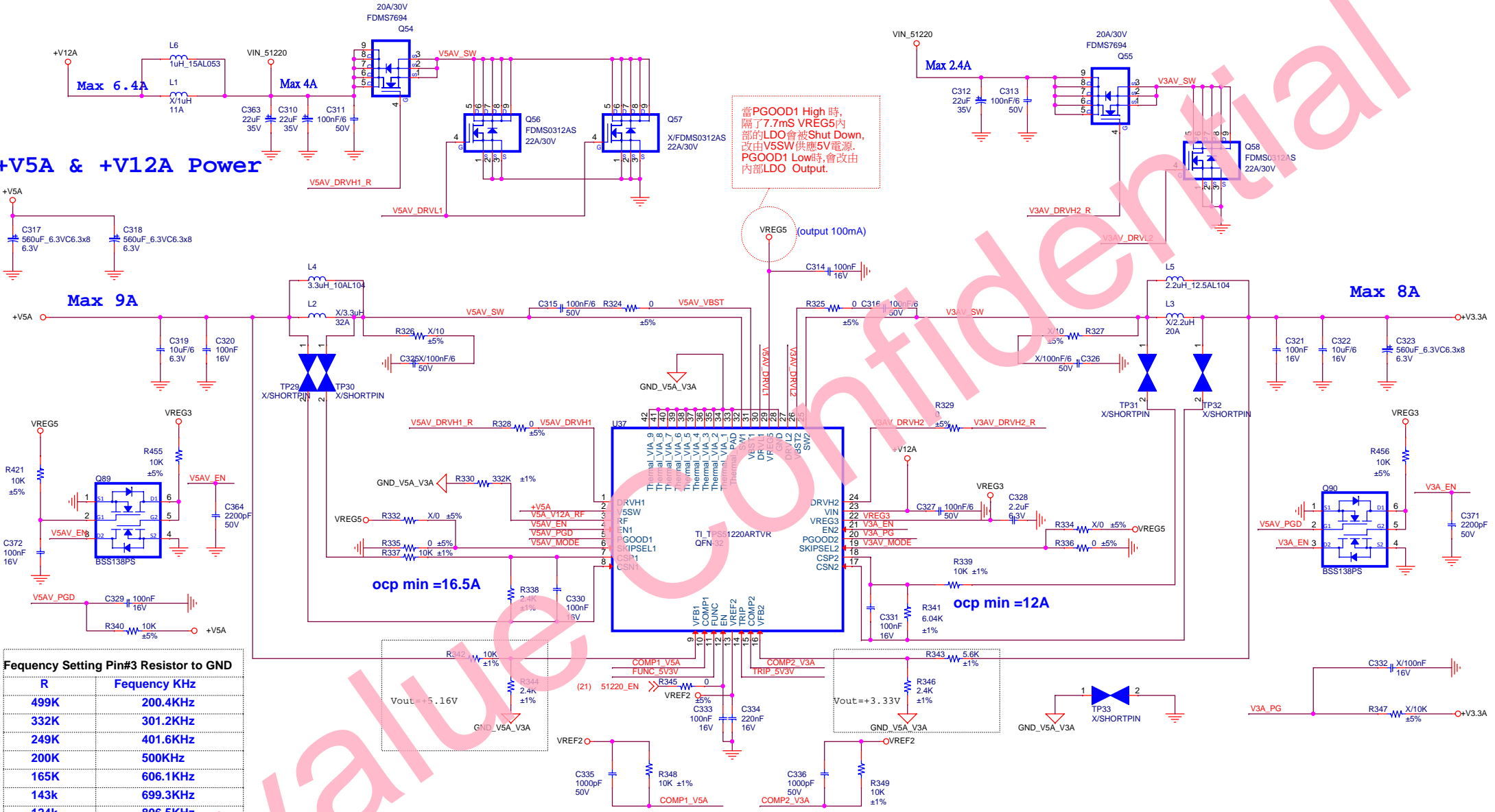
Project Name: REV-Q703

Module Number: <Module no.>

Size A3 Title: V12S,V5S,V3.3S/G Sensor/CAN Rev B1

Date: Thursday, February 09, 2017 Sheet 19 of 26

+V5A & +V12A Power



當PGOOD1 High時，隔了7.7ms VREG5內部的LDO會被Shut Down，改由V5SW供應5V電源。PGOOD1 Low時，會改由內部LDO Output。

ocp min =16.5A

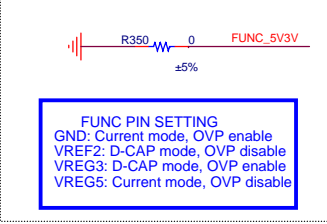
ocp min =12A

Frequency Setting Pin#3 Resistor to GND

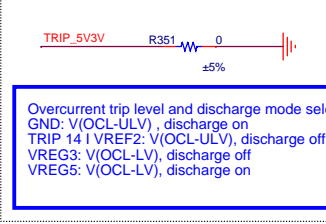
R	Frequency KHz
499K	200.4KHz
332K	301.2KHz
249K	401.6KHz
200K	500KHz
165K	606.1KHz
143k	699.3KHz
124k	806.5KHz
110K	909.1KHz
100K	1MHz

SS time Setting EN1,2 pin cap		MODE 1,2 SELECT	
X	Standard 0.96mS	GND	Continuous conduction mode
2200pF	1.1mS	VREG2	Auto Skip
3600pF	1.8mS	VREG3	Auto Skip, maximum 7 skip (suitable for FSW< 400KHz)
5600pF	2.8mS	VREG5	Auto SKIP, maximum 15 skip (suitable for equal to or greater than 400KHz)
8200pF	4.1mS		

12 PIN Setting



14 PIN Setting



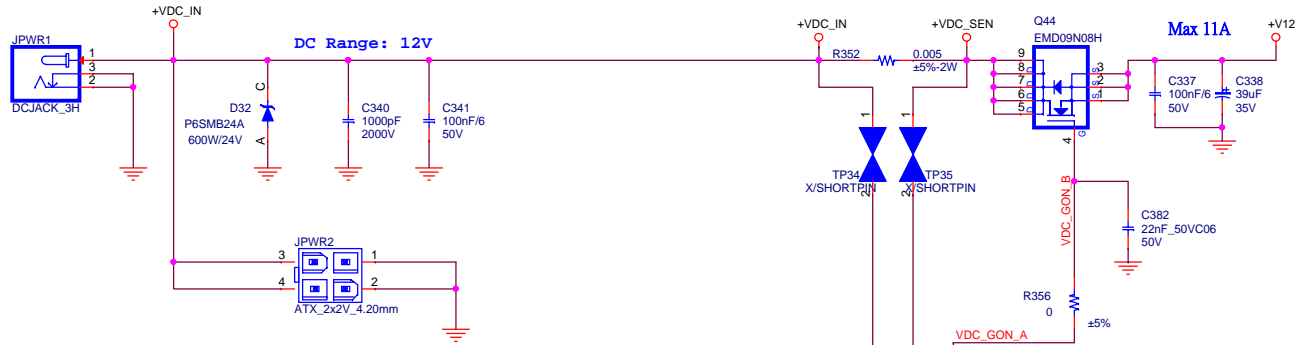
<Variant Name>

Confidential

Project Name	REV-Q703	Module Number	<Module no.>	Rev	?
Size A3	Title	TPS51220A +V5A & +V3.3A		Rev	B1
Date:	Thursday, February 09, 2017	Sheet	20	of	26

VDC-In Protection

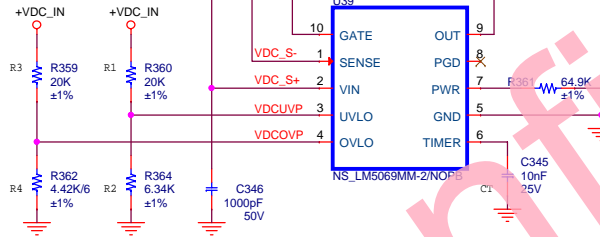
If RS = 5mohm,
 I LIM(min) is 9.7A
 I LIM(typ) is 11.1A
 I LIM(max) is 12.3A



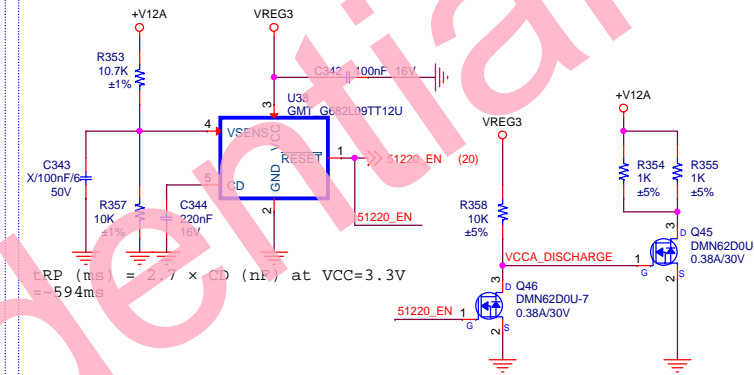
VDC-In OVP/UV Protection

R3 = 20K, R4 = 4.75K
 V OV is 13.25V ~ 14.36V

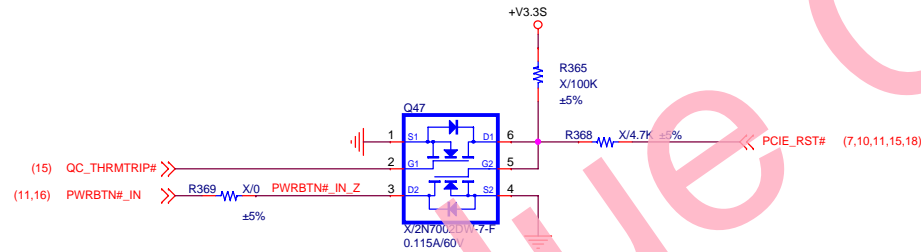
R1 = 20K, R2 = 5.9K,
 V UV is 10.1V~10.59V



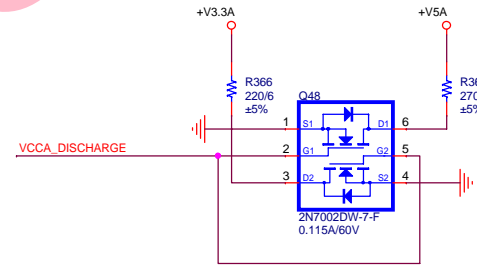
防瞬断放电



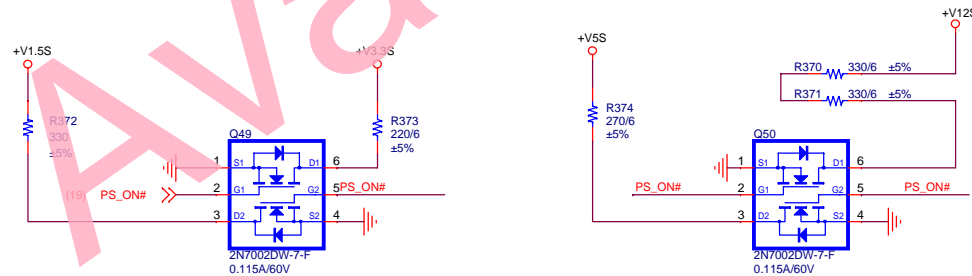
If 'THRMTrip#' goes active the system immediately transitions to the S5 State



VCCA discharge

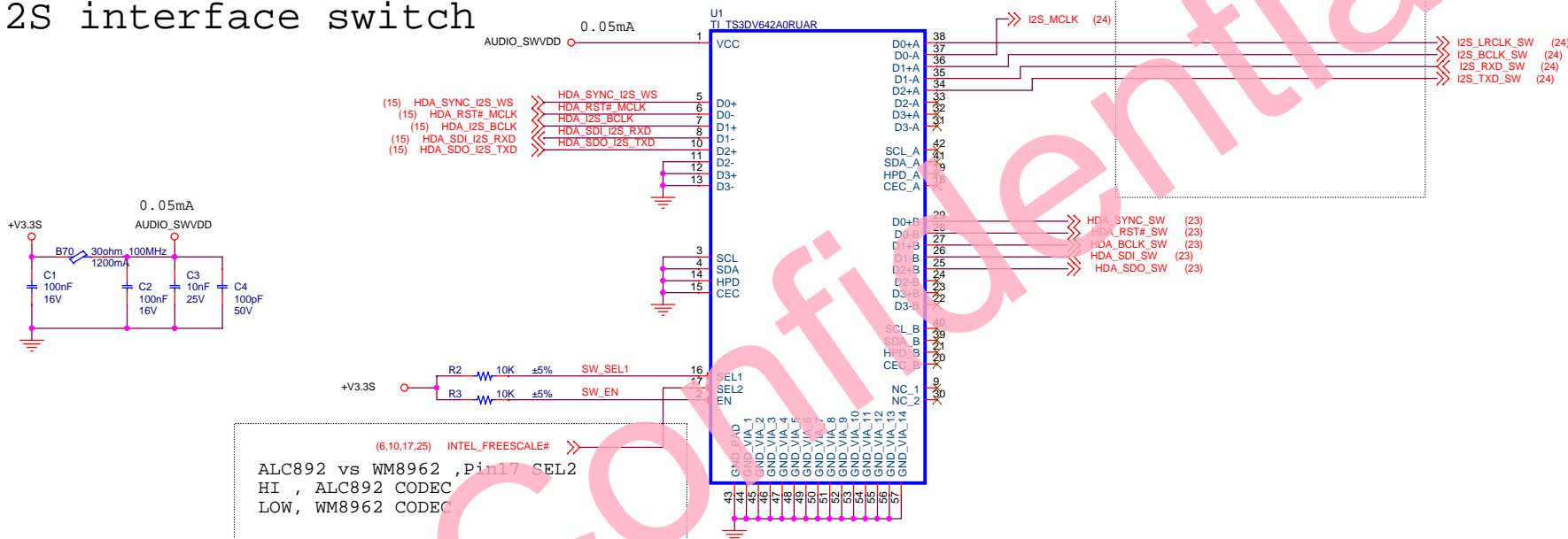


VCC discharge



Del R468,Q81
 Remove C378,C379,R467
 Changed R26,R27,R28 from 0ohm to 22ohm.

HDA & I2S interface switch



EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0- to D0+A/D0-A ON. All the other channels Hi-Z.
H	L	H	D0+/D0- to D0+B/D0-B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

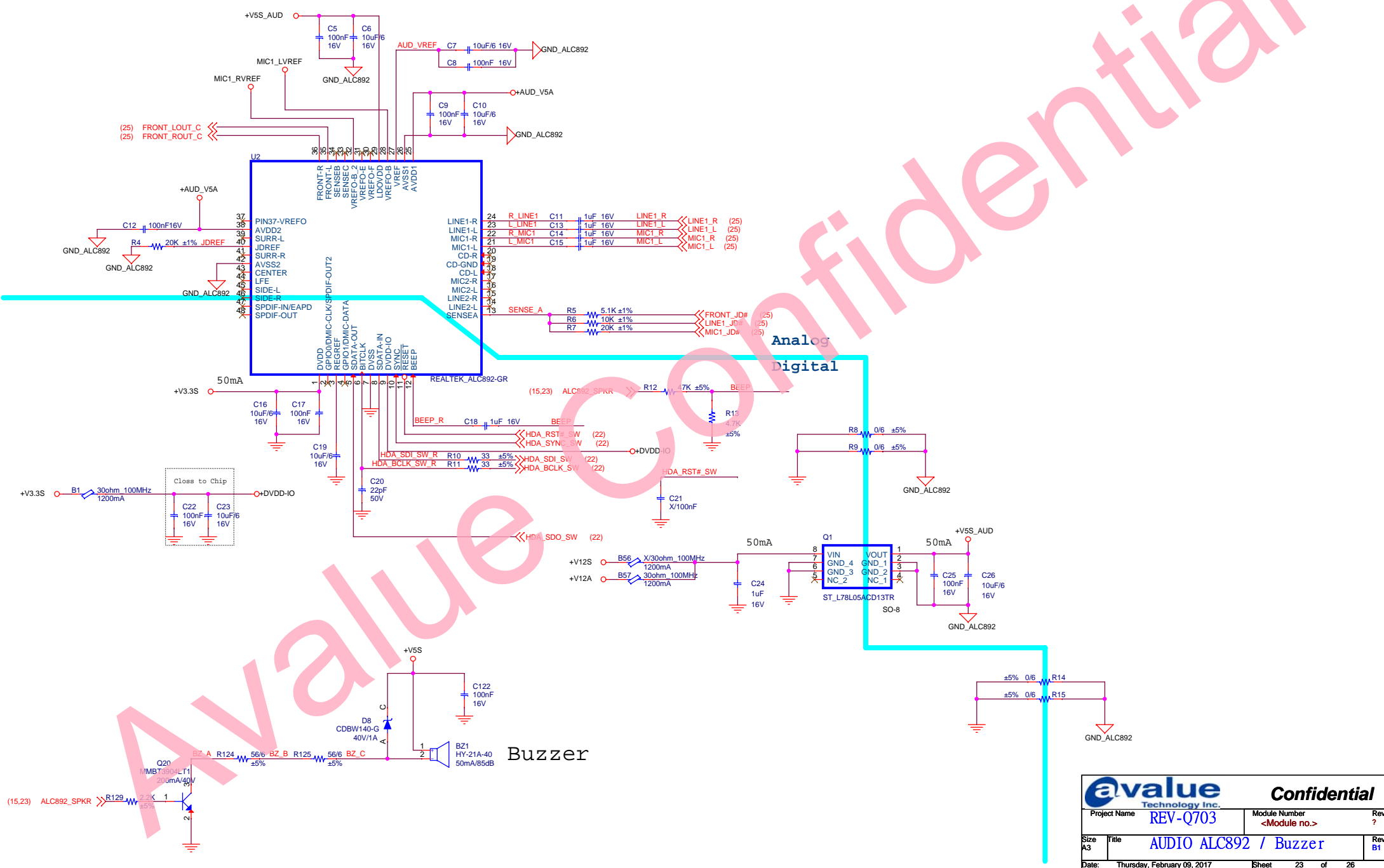
Use all channel.

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Project Name: REV-Q703 Module Number: <Module no.> Rev: ?

Size: A3 Title: HDA & I2S Switch Rev: B1

Date: Thursday, February 09, 2017 Sheet: 22 of 26



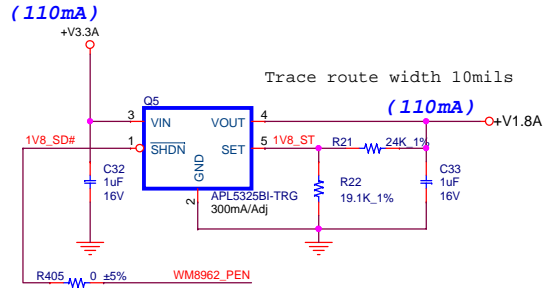
Analog
Digital

Buzzer

		Confidential	
Project Name	REV-Q703	Module Number	<Module no.> ?
Size A3	Title	AUDIO ALC892 / Buzzer	
Date:	Thursday, February 09, 2017	Sheet	23 of 26

+V1P8 POWER

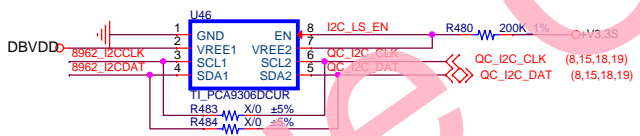
Trace route width 10mils



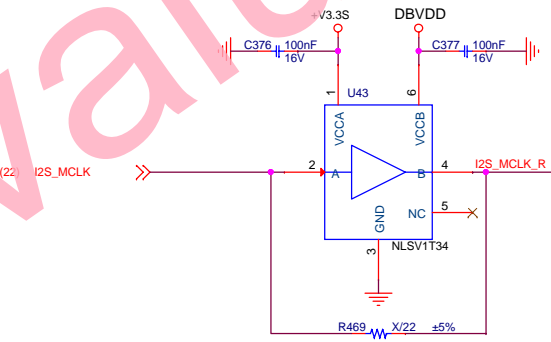
LDO:VCC3P3 to VCC1P8 - 1.1mA

$V_{out} = 0.8 [1 + (R_{up}/R_{dn})]$
 $= 1.805V$

Rdn recommended value is in the range of 100 to 100k.



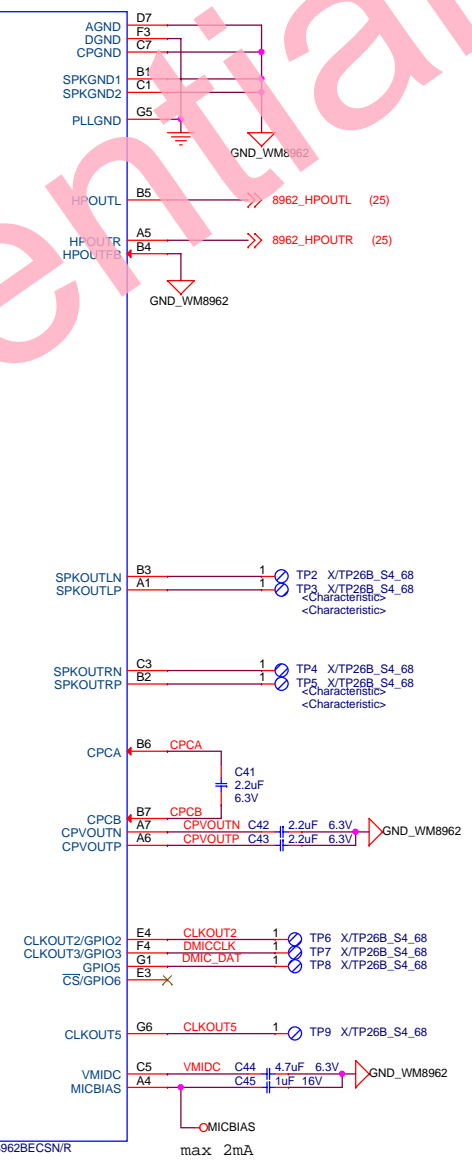
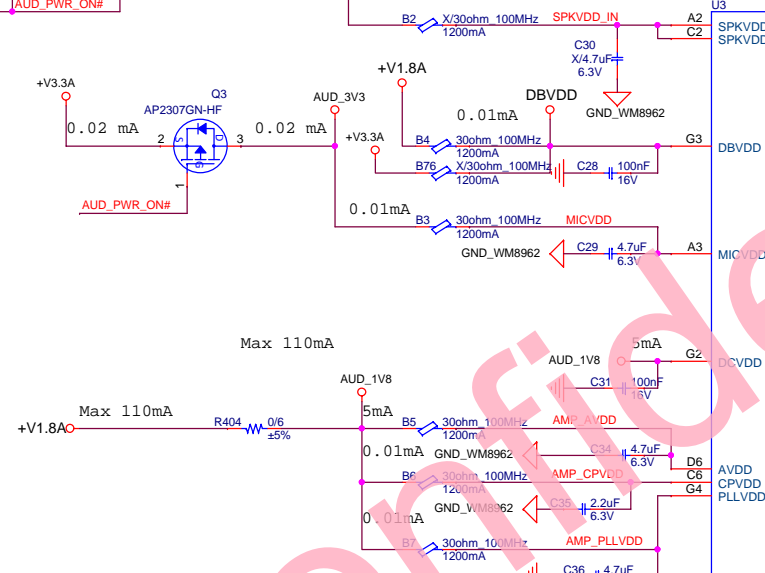
VREF1 Low-voltage-side.
 VREF2 Hi-voltage-side.



- (22) I2S_BCLK_SW
- (22) I2S_LRCLK_SW
- (22) I2S_TXD_SW
- (22) I2S_RXD_SW

SPKVDD1, SPKVDD2=+5V
 DCVDD, AVDD, PLLVDD, CPVDD=+1.8V
 MICVDD, DBVDD=+1.8V

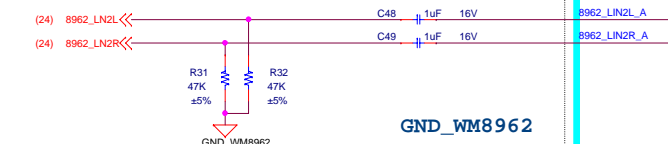
Max 800mA when driver per CH 2W
 Max 50mA when driver per CH 0.1W(暫定選用)



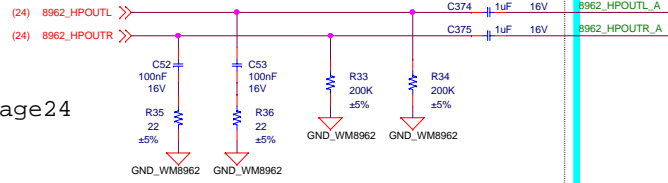
Variant Name:

		Confidential	
Project Name	REV-Q703	Module Number	<Module no.>
Size A3	Title	AUDIO WM8962	
Date:	Thursday, February 09, 2017	Sheet	24 of 26

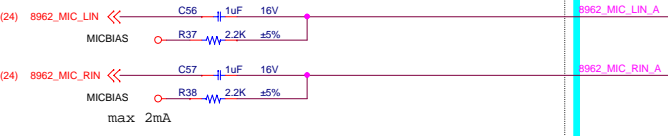
LINE IN



LINE OUT

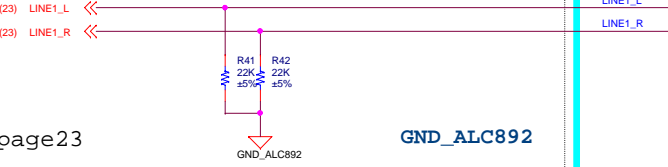


MIC



From WM8962
Placed on page24

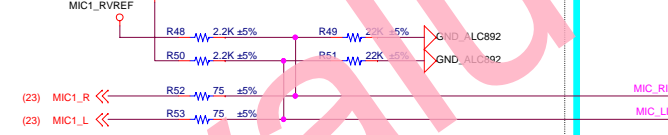
LINE IN



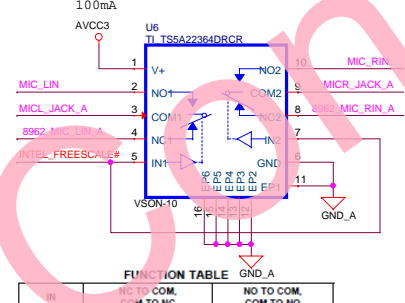
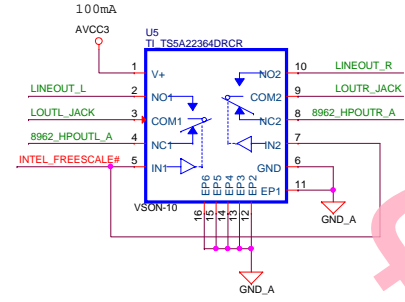
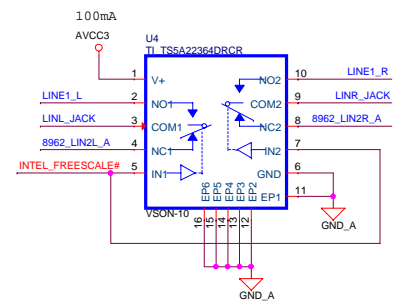
LINE OUT



MIC



From ALC892
Placed on page23



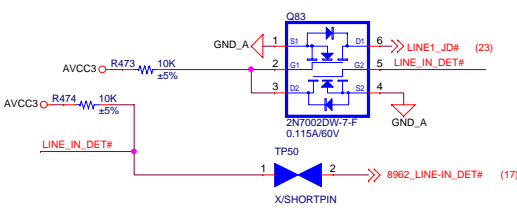
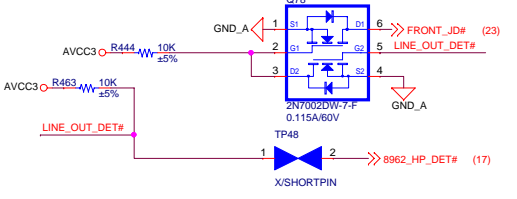
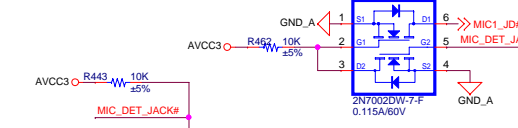
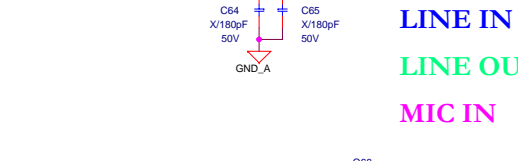
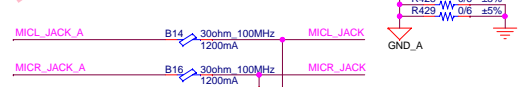
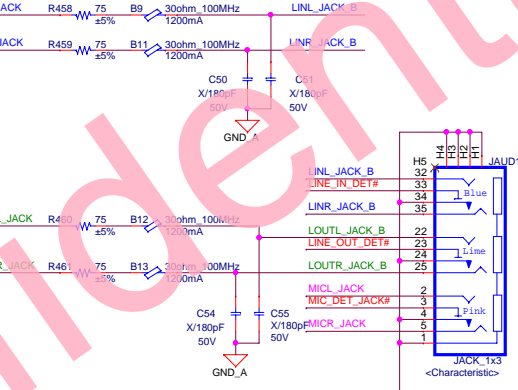
FUNCTION TABLE

IN	MIC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

(6,10,17,22) INTEL_FREESCALE#
ALC892 vs WM8962 ,
HI , ALC892 CODEC
LOW, WM8962 CODEC

$$V_{out} = 0.8 [1 + (R_{up}/R_{dn})] = 3.328V$$

Rdn recommended value is in the range of 100 to 100k



Reversion History List:

REV-Q703 Ver:A0

EE :Dasmon Yang

Item	Description	Track or reason	Page	Date
0	Apply new P/N E1907Q70300RO-W1 ; E9697Q70300R ; E9695Q70300R	First Release	1	2014/09/18

REV-Q703 Ver:A0->A01

EE :Dasmon Yang

Item	Description	Track or reason	Page	Date
0	Apply new P/N E1907Q70301RO-W1 ; E9697Q70301R ; E9695Q70301R	2nd Release	1	2014/11/14
1	Add C374-C379 , R458 ~R461, Changed all luf/0603/MLCC to 0402 type.	Adjust Analog volt level	25	2014/11/14
2	Changed L1 from E121220102BH to E1212201020H.	CIS footprint error	20	2014/11/14
3	Remove R44,R45,R39,R40,R46,R47	Adjust Analog volt level	25	2014/11/24
4	Changed R352 to E10187005CXH (0.005 ohm/5%) R361 change to 64.9K_1%(E1051564921H)	Adjust Vin R sense. Setting to Mosfet Watt.	21	2014/11/26
5	R341 changed to 6.04K_1%(E1050560410H)	Setting Iccp Point	20	2014/11/26
6	Del Y1, Add OSC1 ,R457 , C373	CLOCK issue	24	2014/12/11
7	Changed C200, C347, C317, C318 and C323 to 5k hours of life cycle		20, 11	2015/1/6
8	Changed U27 to E1489811500H	At mode on/off issue	16	2015/1/7
9	Changed R287 to 10.7K/0402/1%	At mode on/off issue	18	2015/1/8
10	Add Q79, Q80, R465	SD card boot issue	8	2015/1/8
11	Changed B4 connector to +V1.8A instead of +V3.3A. Changed R33,R34 to 200k/0402.		24	2015/1/21

REV-Q703 Ver:A01>A1

EE :Dasmon Yang

Item	Description	Track or reason	Page	Date
0	Apply new P/N E1907Q70302RO-W1 ; E9697Q70302R ; E9695Q70302R	3rd Release	1	2015/4/13
1	Del R468,Q81 ; Remove C378,C379,R467 ; Changed R26,R27,R28 from 0ohm to 22ohm ; Add U46,R480	WM8962 level shift issue.	22,24	2014/11/14
2	Changed R276 from 4.7K to 100K.	HW issue	16	2014/11/14
3	Removed C388,C389,Q11,Q12 ; Add U45,R479	HW issue	6	2015/06/01
4	Add R481,R482	HW issue	9	2015/06/10
5	Del U44	HW issue	22	2015/06/29

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Item	Description	Track or reason	Page	Date
0	Changed C384-C387 from 15pf to 0ohm. Changed R475-R478 from 330ohm to 402ohm.	EMI solution	6	2015/8/4

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Item	Description	Track or reason	Page	Date
0	Changed R29(E1051700001H) to 0.luf/0603 (E1127510410H),pre-scan pass.	EMI solution	24	2015/12/24

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Item	Description	Track or reason	Page	Date
0	Add JEDP1 connector , Changed JUSB1 to TWO USB 3.0 connector.	Q7 SPEC update to 2.1	7,13	2016/6/23

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Item	Description	Track or reason	Page	Date
0	R227 R228 R229 R230 R231 changed to 0ohm. Add R497 short to GND, (Add R500,R501 co-layout) Q44 EOL so change to new part.	HW ISSUE	15 21	2017/01/23 2017/01/23
1	Q5, Q29, Q67 EOL change to new part ,		24,25,14	2017/02/09

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